UNIVERSITY OF CAPE TOWN

DSP PHASE ANGLE CONTROLLED THREE PHASE TO SINGLE PHASE UNINTERRUPTIBLE POWER SUPPLY

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DECLARATION

The author declares that this thesis has not been submitted before at any university. The author hereby confirms that it is based on his work.

Caxton Magozore

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The author's sincere gratitude goes to the following people for invaluable contribution towards this project:

- Mr M. Malengret, thesis supervisor for his support and making this project a success.
- UCT power electronics group, Johan, Clint, Ben, Paul, and my friend Chris Ndoro who were always ready and willing to help.
- Mr C. Hozniak, technical staff, who was always there for assistance.
- Lastly my family for their support.

TERMS OF REFERENCE

Mr Malengret, Senior Lecturer in the Electrical Engineering Department, commissioned this project at University of Cape Town. He also supervised it in fulfilment of the requirements of MSc Degree in Electrical engineering.

The main objective was to design, build and test a DSP Phase Angle Controlled Three to Single Phase UPS System according to the following specific terms:

1. Generate Space vector PWM pulses for inverter switching.

2. Phase lock the inverter output to the mains and use phase angle technique to charge batteries and regulate the dc bus.

3. UPS to draw sinusoidal balanced currents from the mains supply.

4. Draw power at close to unity power factor from the supply.

5. Regulate the output voltage during both battery charging and battery discharging mode.

Synopsis

Power reliability is business reliability. Today's industrial trend of using sophisticated electronic equipment to increase productivity, quality and efficiency in the work place has further compounded power reliability issues. The electronics utilised by most industrial equipment today are becoming increasingly sensitive, even to minor power disruptions. Also the proliferation of these electronic equipment has resulted in the "pollution" of the ac mains in the form of unwanted harmonics.

Large power supplies in industries are three-phase supplies. Therefore single-phase electronics equipment such as workgroup file servers, data processing computers, sensitive lab equipment and computer clusters have to be equally distributed on the three phases, to keep the phases balanced. Equal distribution of the loads on the three phases is not easily achieved all the time.

In critical applications power supply abnormalities are unacceptable. Backup of the utility grid is provided by an Uninterruptible Power supply (UPS). The UPS acts as a buffer. It provides clean and reliable power to the vulnerable loads, under any normal or abnormal power supply conditions.

Today's low-cost, high-performance digital signal processor (DSP) controller provides an improved and cost effective solution for the UPS design. . Multiple control algorithms are executed at high speed enabling high sampling rate for good dynamic response.

This thesis presents a new component minimised line-interactive DSP controlled UPS design. The topology provides load balancing. It draws balanced power from a three-phase utility and supplies it to a single-phase load. The topology was chosen for its desirable characteristics of high efficiency, high reliability, simple circuit and low cost. At the same time providing a good isolation from most power line problems.

The UPS is inverter based. Space vector modulation technique is used for the inverter switching. The inverter output is phase locked to a three-phase supply and is linked to the three-phase supply through link inductors. Power flow through the link inductors is controlled by controlling both the magnitude and phase angle of the inverter output,

relative to the incoming mains. The amount of power that flows and the stability of the system is determined by the size of the linking inductors and the phase shift angle. A compromised solution of the linking inductor size and the phase shift angle is needed to have a stable system, good power factor and to fulfil all the objectives of the UPS.

The operating principles of the proposed UPS are based on Enjeti, Jae-Ho Choi and Feng approaches. The operating principles of the proposed UPS were illustrated with a simplified single-phase equivalent circuit. Matlab simulink was used to simulate the equivalent circuit. With a full understanding of the operating principles of the UPS a mathematical simulation method was then developed. The mathematical simulations that was carried out produced results identical to the simulink results. Using mathematical simulations, variables could be easily changed and the power flow diagrams plotted. By varying the different variables and plotting the power flow diagrams a compromised solution is reached. The calculated values were then simulated on a three-phase system using matlab simulink.

To validate the theory and simulations results a 2.5kVA laboratory UPS prototype was built. Four sensed signals were used to implement a closed loop control of the UPS using a TMS320F243 DSP board. The results showed a successful implementation of the proposed DSP phase angle controlled three to single phase UPS.

It was concluded that the UPS provides load balancing and a good solution to most power line problems. Although the test done showed a successful operation of the UPS, it was recommended for future research to take more tests at higher power rating. It was also recommended to investigate the dynamic response of the UPS to different electrical faults.

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1 INTRODUCTION

Uninterruptible Power Supply (UPS) is a device that operates between the utility and a load. The function of the UPS is to act as a buffer and provide clean and reliable power to vulnerable loads under any normal or abnormal power supply condition. The basic concept of UPS is to store energy during normal operation through battery charging and release energy through dc to ac conversion during power failure or power outage.

Power reliability is business reliability. Traditionally UPSs were only used in critical application such as PC, communication and life supporting equipment. In today's economy, uninterruptible power supplies are widely used. They are adopted also for less critical loads such as home offices.

Power reliability issues are further compounded by a general industrial trend of using more sophisticated electronics equipment to increase productivity, quality and efficiency in the work place. The electronics utilised by most industrial equipment today are becoming increasingly sensitive, even to minor power disruptions [13]. In addition proliferation of these electronic devices has resulted in the "pollution" of the ac mains in the form of unwanted harmonics. It has therefore become important that the quality of the current drawn from the supply do not exasperate the problem.

Most power supplies in industries are three-phase systems because the three-phase has more advantages over single-phase power transmission. Single-phase loads such as workgroup file servers, data processing computers, sensitive lab equipment, telecom equipment and computer clusters have to be equally distributed on the three phases, so as to keep the phases balanced. Equal distribution of the loads on the three phases is not easily achieved all the time. This then creates a need for a three to single phase conversion system for medium size loads typically in the range of 6kVA to 20kVA.

Among various UPS topologies or configurations on-line UPS (explained in detail in chapter two) offers good line-conditioning performance and good protection to the loads against any utility power problems. However, because of the use of multiple power conversion stages, the UPS is complex, expensive, has low efficiency and low reliability [14].

Line-interactive UPS topology combines the performance benefits of the on-line UPS with the reliability and efficiency benefits of the standby UPS also explained in detail in chapter two.

Since everyone needs to keep his or her business up and running, it is important to have a cost-effective UPS design that is affordable. The UPS should also eliminate the problem of unbalanced single-phase loads, and not generate distortions on the utility.

Today's low-cost, high-performance DSP controller provides an improved and cost effective solution for the UPS design. . Multiple control algorithms are executed at high speed enabling high sampling rate for good dynamic response [14].

This thesis sets out the investigation of the viability of a new component minimised line-interactive DSP controlled UPS design. The UPS has a three-phase input and single-phase output. The topology has an ability to draw balanced power from a three-phase utility and supply it to a parallel combination of single-phase loads.

The topology was chosen because of its desirable characteristics of high efficiency, high reliability, simple circuit and low cost. At the same time providing good isolation from most power line problems.

1.1 Historical Background

Introduction

Ideally the voltage supplied by the utility system should be a perfect sine wave without any harmonics at its nominal magnitude and frequency. Figure 1-1 shows a perfect sine wave at 50Hz from a function generator. In practice, however voltages can significantly depart from the ideal conditions due to the power line disturbances. Abnormalities such as over voltage, under voltage (brown out), outage (blackout), voltage spikes, chopped voltage waveform, harmonics, and electromagnetic interference must be mitigated [4].

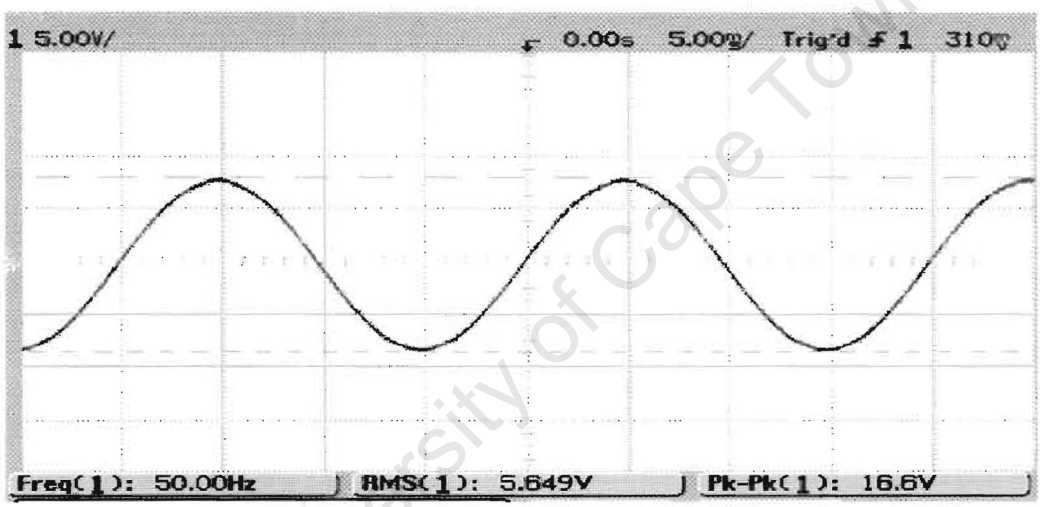

Figure 1-1: Perfect sine wave from a function generator

Sources that produce disturbances are very diverse. For example in a city like Harare summer rains are associated with lightening. During this time short-circuit faults are prominent in power systems when equipment insulation fails due to system over voltage caused by lightning [12].

Figure 1-2 shows a typical University of Cape Town (UCT) utility voltage (line to neutral) sine wave characterised by a flat top. Such waveform problem is often the case where a large number of computers are supplied.

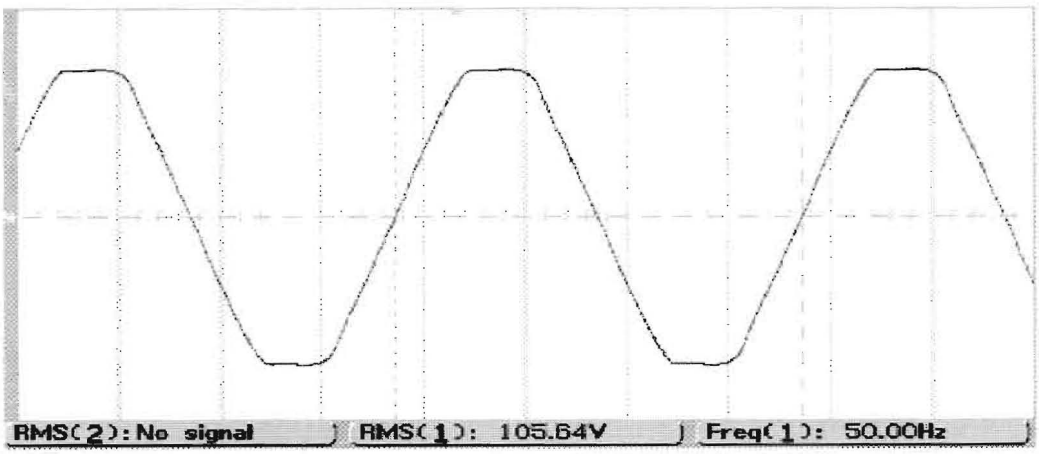

Figure 1-2: UCT voltage waveform

The effects of such power line disturbances on sensitive equipment depend on the type of equipment. The way some equipment responds to an outage can greatly increase down time. Some equipment have instant restart on power return, some have auto restart after a time delay and others need human intervention for a manual restart.

In cases where applications are critical such disturbances are unacceptable. The backup of the utility grid is provided by an Uninterruptible Power supply (UPS). The UPS acts as a buffer and provides clean and reliable power to the vulnerable loads.

UPS Techniques have developed rapidly. Recent UPSs make use of DSP technology, which is a type of a microprocessor that is used for control algorithms of the UPS. DSP is appropriate because it is fast and effective in processing data in real time. The real time capability makes DSP ideal for applications that cannot tolerate any delays. The real time performance, flexibility, increased system performance and reduced system cost makes it superior to other microprocessors.

Different authors have researched on an extensive range of UPS topologies. Here is a brief summary of conclusions and recommendations from the investigations on UPSs that were previously undertaken at University of Cape Town.

1.1.1 Supply-friendly Single Phase UPS

Investigation on the possibility of modifying locally manufactured UPS to meet certain design specifications was carried out. The main short fall was processing power, precluding the use of floating point or an optimal control algorithm, which ultimately compromises the performance of the system. The author of supply-friendly single phase UPS recommended a 16-bit micro-controller or low-end digital signal processor (DSP) to provide extra processing power needed to optimise the UPS response [1].

1.1.2 Three to Single Phase UPS Implementing Space Vector PWM Technique Using DSP

On-line three-phase to single-phase UPS system, which is based on Enjeti and Jae-Ho Choi and Feng approaches was investigated. The control algorithm was done using Motorola DSP56002. The DSP was programmed in assembler language which is a low-level language making it difficult to have a compact code. It was difficult to have a phase error of less than one degree when using zero crossing method for phase locking. The author of the thesis referenced below had difficulties implementing the phase shifting method for power flow control. The system was not stable. It was however concluded that using the correct phase shift angle range and inductor values, successful control could be achieved [2].

1.1.3 DSP controlled Three Phase to Single Phase UPS

Same topology as above was investigated. A DSP development kit, MSK243 from technosoft S. A. Switzerland which is based on the Texas Instrument TMS320F243 motor control was used for control.

The author of the thesis referenced below programmed in C-programming language, and found it necessary to write the bulk of the program using fixed-point routines. That made the writing of the program much more challenging. Most of the processing capacity of the DSP was needed to implement phase locking and space vector modulation routines. The author suggested for an alternative solution to be found to

1.2.4 The proposed UPS Topology

The same topology as proposed above was investigated by the author with an aim of circumventing the problems experienced, and to ensure that the objectives of the project were achieved without compromising on the functionality of the UPS. The schematic diagram of the proposed topology is illustrated in figure 1-3 below. New system hardware, software and control method is presented using a TMS320F243 DSP board. The validity of the proposed strategy is demonstrated by means of simulations and experimental results referring to a built (2.5 kVA) three to single-phase laboratory UPS prototype.

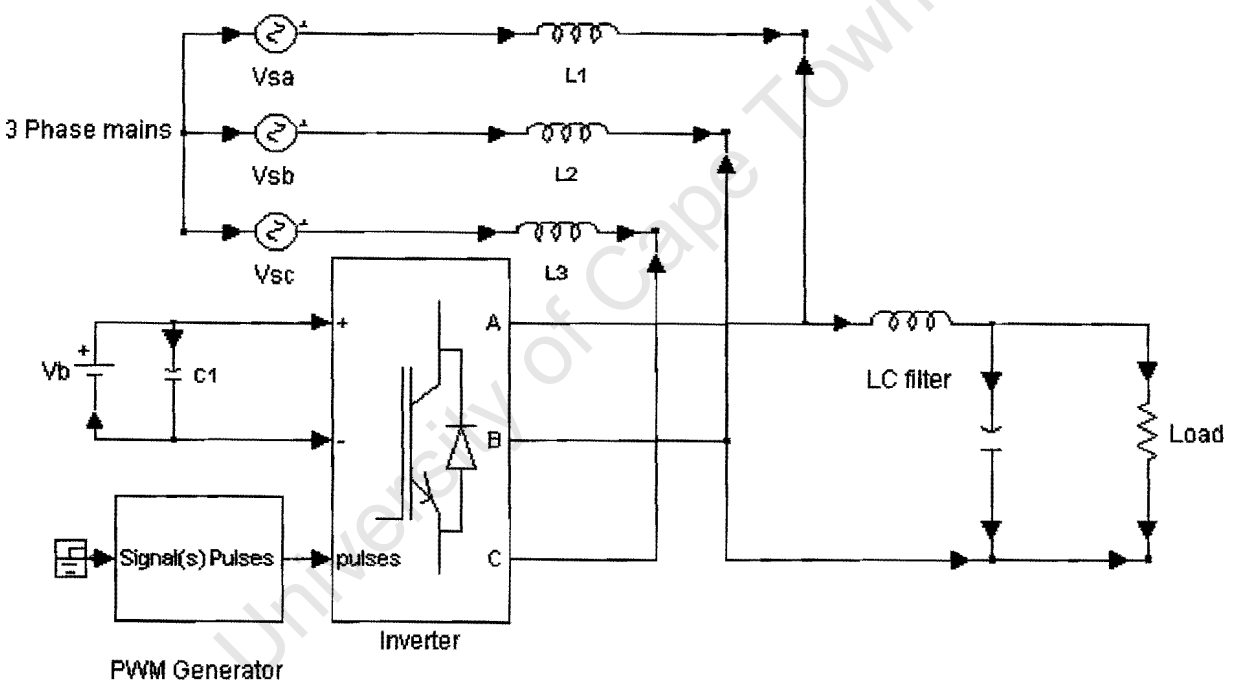

Figure 1-3: The schematic diagram of the proposed UPS Topology

1.2 The objectives of the report

The thesis presents the results of the building and testing of the proposed online phase angle controlled Three Phase to Single Phase UPS system.

The objectives of the report were:

1. To generate PWMs using Space Vector Modulation Technique for inverter switching.

2. To phase lock the inverter output to the mains and to use phase angle technique to charge batteries and regulate the dc bus. Phase angle technique is a method of controlling power flow through link inductors. This is achieved by controlling both the magnitude and phase angle of the inverter output, relative to the incoming mains [10].

3. UPS to draw sinusoidal balanced currents from the mains supply.

4. To draw power at close to unity power factor from the supply.

5. To regulate the output voltage during both battery charging and battery discharging mode.

6. To draw conclusions and recommendations based on the findings of the report.

1.3 Plan of Development

The report begins by discussing merits of UPS topologies commercially available, and the merits of the proposed topology. The theoretical concepts of the proposed topology are then explained in detail. Theory of space vector modulation technique is discussed next. The report then presents the proposed topology simulation results. The hardware and software used for building the laboratory UPS prototype is described. Finally the laboratory UPS prototype experimental results are given. Conclusions and recommendations are given based on the results.

2 LITERATURE REVIEW OF UNINTERUPTIBLE POWER SUPPLIES

2.1 Introduction

It is widely believed that there are two types of UPS systems, namely standby UPS and on-line UPS. These two names do not correctly describe many of the UPS topology available [5]. There are different UPS topologies commercially available each with different merits, but they all have the same primary function of:

Power quality improvement
Back up source of power

Here is a summary of UPS topologies for the reader to have a clear distinction of the proposed system from other UPS topologies. Note that the solid line represent the primary power path of the UPS [5].

Standby Uninterruptible Power Supply

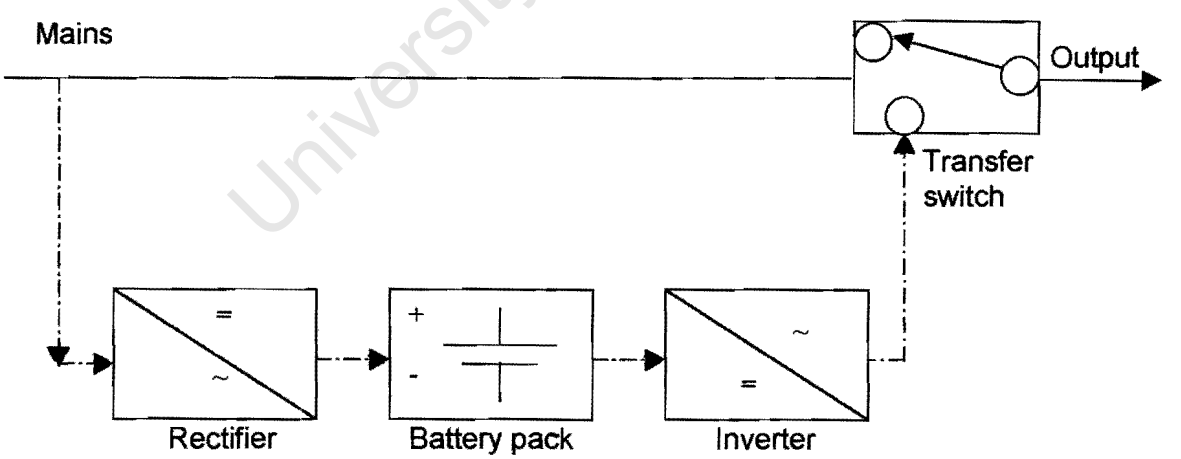

Figure 2-1: **Conventional Standby UPS Topology**

Standby UPS is shown in figure 2.1, the mains power line directly supplies power to the load, until power fails. Then a battery-powered inverter turns on and continues supplying power to the load. This type of supply is sometimes called an offline UPS. Batteries are charged as necessary when line power is available. The quality and effectiveness of this class of devices vary considerably [5].

Advantages of Standby UPS

- They are generally cheaper than the online UPS. Since the appliances connected to the supply are basically connected to the mains power line.
- Small size and high efficiency.

Disadvantages of Standby UPS

- Standby UPS provide relatively poor protection from line noise, frequency variations, line spikes and brownouts.
- There is a transfer time of switching to the inverter when the mains fail.

2.3 Standby On-Line Hybrid UPS

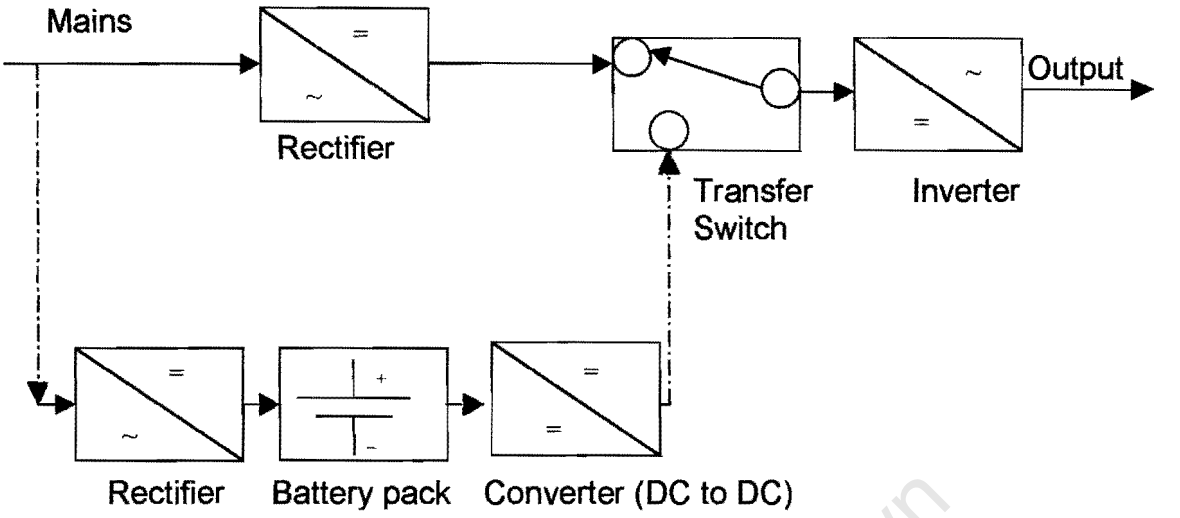

Figure 2-2: Conventional Standby On-Line Hybrid UPS Topology

Standby On-Line Hybrid UPS, Figure 2.2 The standby DC to Dc converter from the battery is switched on when an AC power failure is detected just like in the standby UPS. The power path from the battery to the output only the inverter is on-line, while the dc to dc converter is operated in the standby mode [5].

Advantages of Standby On-Line Hybrid UPS

- The UPS provide the best isolation from the power line problems.
- UPS exhibit no transfer time during an AC power failure.

Disadvantages of Standby On-Line Hybrid UPS

- Efficiency is low due to the presence of four power converters.
- The UPS cost per VA is high.
- Low reliability

2.4 Standby-Ferro UPS

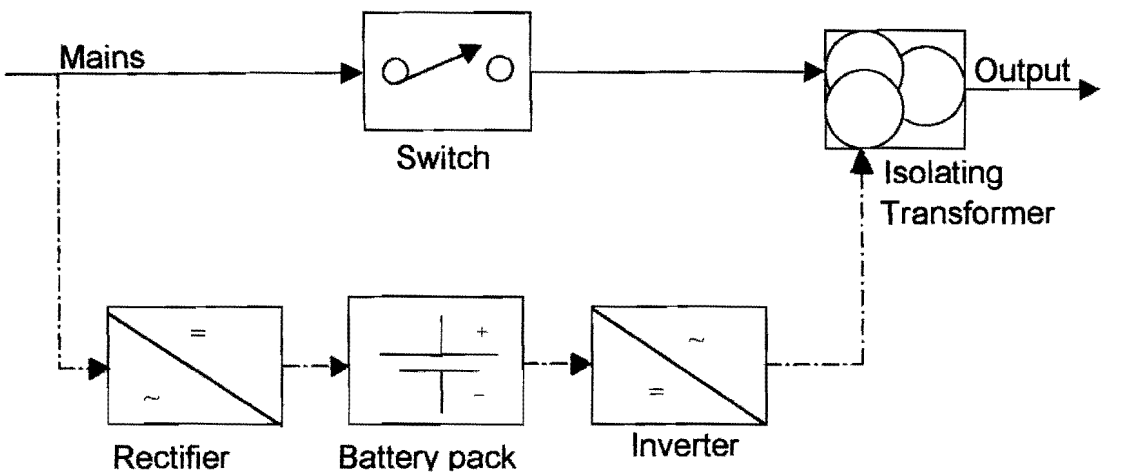

Figure 2-3: Conventional Standby-Ferro UPS Topology

Power is supplied from AC mains through a transfer switch, through a saturating transformer that has three windings, and to the output as shown in figure 2.3 above. In case of power failure the inverter picks up the output load [5].

Advantages of Standby-Ferro UPS

- It provides good protection against line noises.
- It maintains output on its secondary briefly when a total outage occurs.
- High reliability.

Disadvantages of Standby -Ferro UPS

- Increased cost and increased power consumption.
- Low efficiency due to heat generated by the Ferro-transformer.

2.5 Line Interactive UPS

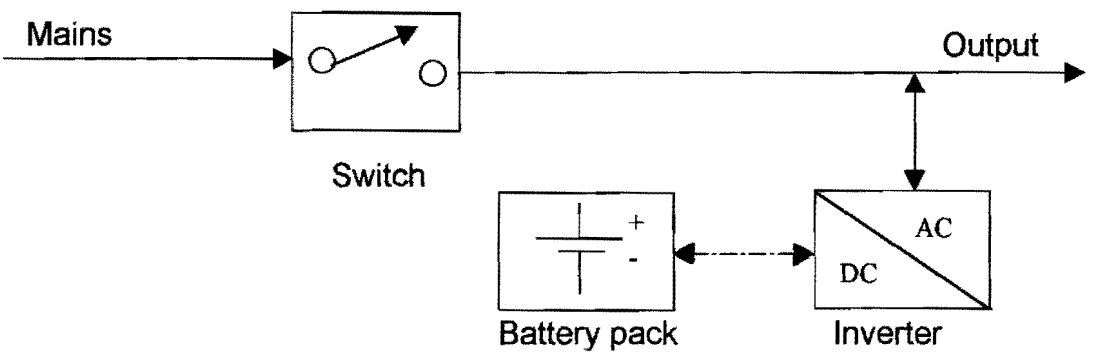

Figure 2-4: Configuration of Line interactive UPS Topology

Line interactive UPS illustrated in figure 2.4. The inverter is always connected to the output of the UPS. During normal operation (when there is power from the mains), power is supplied to the load from the mains, and the inverter is operated in reverse at low power to charge the battery set. On mains failure, the transfer switch is opened to stop power flowing from the inverter to the mains. The topology combines the performance benefits of the online UPS with the reliability and efficiency benefits of the standby UPS [5].

Advantages Line-interactive UPS

- It does not have transferring time.
- It regulates output voltage during normal operation and when mains fail.
- This topology is inherently very efficient which leads to high reliability while at the same time proving superior protection from the power line problems.

Disadvantages of Line-interactive UPS

- There are filtering and switching losses involved although these losses are much less than losses in the conventional standby UPS.

2.6 Double Conversion On-line UPS

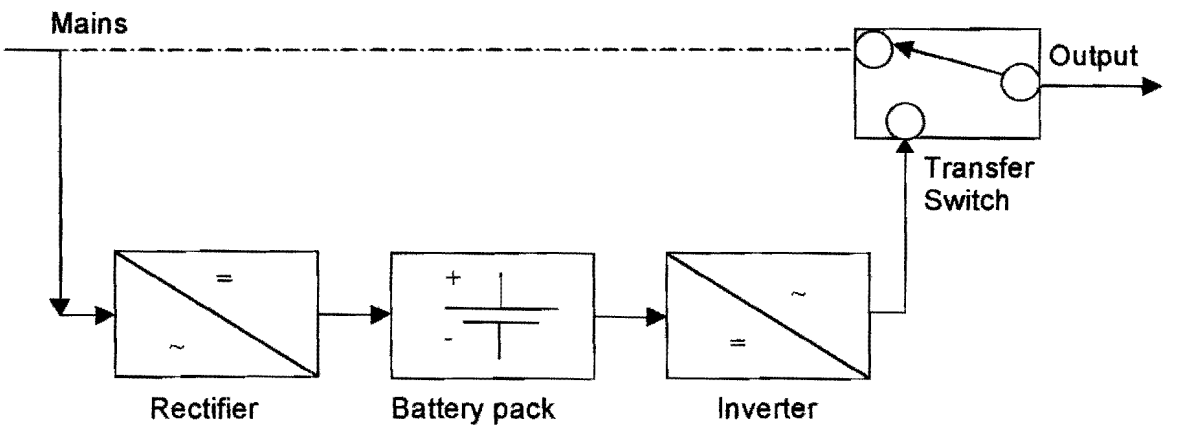

Figure 2-5: Double Conversion On-line UPS Topology

The configuration of the double conversion on-line UPS topology is the same as the standby. The only difference is the primary power path of the AC mains. In double conversion the AC mains is first converted to DC then the inverter converts it back to AC as illustrated in figure 2.5. AC mains is not the primary power source but rather a backup for the UPS [5].

Advantages of Double Conversion On-line UPS

- The UPS provide the best isolation from the power line problems.
- High voltage conditioning.
- It does not have transferring time.

Disadvantages of Double Conversion On-line UPS

- Reduced reliability and efficiency
- Power drawn by batteries is often non-linear causing problems with standby generators.

2.7 Delta Conversion On-line UPS

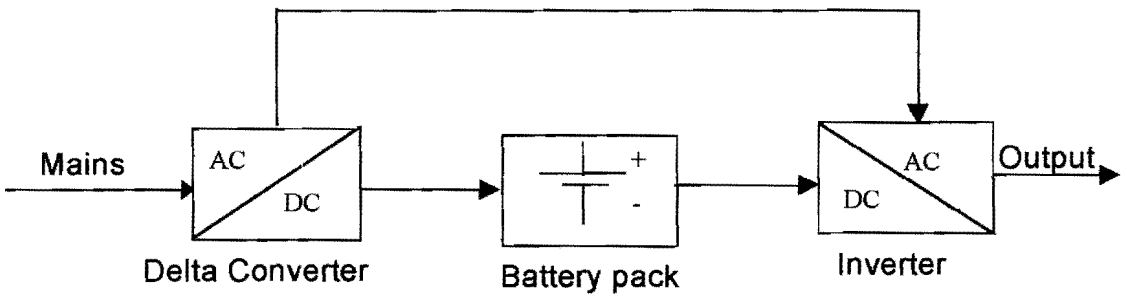

Figure 2-6: Delta Conversion On-line UPS Topology

Delta Conversion On-Line topology illustrated in figure 2.6 was introduced to eliminate drawbacks of the double conversion on-line topology. The inverter supplies power to the load all the time with the delta converter contributing some of the power. When the mains fail power is supplied from the battery pack [5].

Advantages of the Delta Conversion On-Line UPS

- High reliability and efficiency.
- The UPS provide the best isolation from the power line problems.
- Excellent voltage conditioning.

Disadvantages of the Delta Conversion On-Line UPS

- The topology is impractical under 5kVA
- Fairly expensive

2.8 Proposed UPS Topology

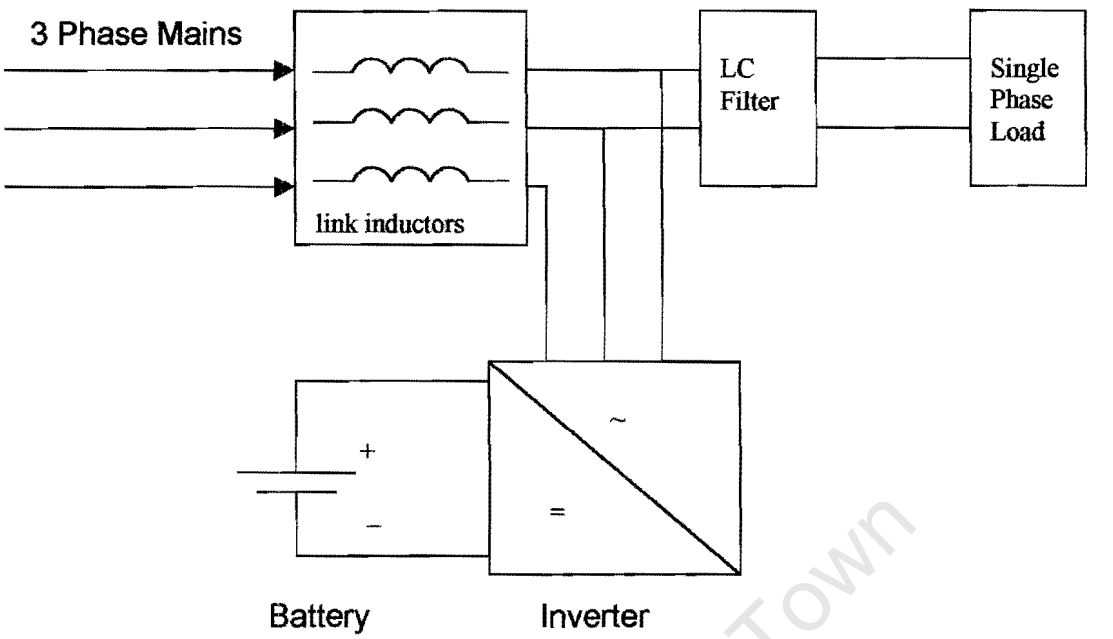

Figure 2-7: The Proposed UPS Topology

The proposed topology is a variation of the line-interactive topology that has been component minimised .It consists of link inductors, and a multifunctional converter, which can work as an inverter and a battery charger bi-directionally.

The advantages of the Proposed UPS Topology

- There is no transfer time on power failure.
- Low implementation cost.
- Capable of operating near unity power factor
- Draws balance power from a three-phase utility supplying single-phase load.
- The UPS provide the best isolation from the power line problems.

Disadvantages of the Proposed UPS Topology

- There are filtering and switching losses involved but less than losses in the conventional standby UPS.
- No galvanic isolation unless a transformer is added to the input or output of the UPS.
- The neutral cannot be grounded.

3 THEORETICAL CONCEPTS OF THE PROPOSED UPS TOPOLOGY

3.1 Introduction

The proposed component minimised UPS topology illustrated in figure 3-1 consists of a three-phase space vector modulated inverter. Which is a converter in the true sense converts power from dc to ac and vice versa. During normal operation, when power is supplied by the utility, the magnitude of the inverter voltage is regulated resulting in a stabilised load voltage independently to the utility voltage. In the meantime the inverter provides a battery charging function as well. The inverter is connected to the utility supply through link inductors [9]. The line harmonic currents are reduced based on the principle that links inductor presents high impedance to harmonics.

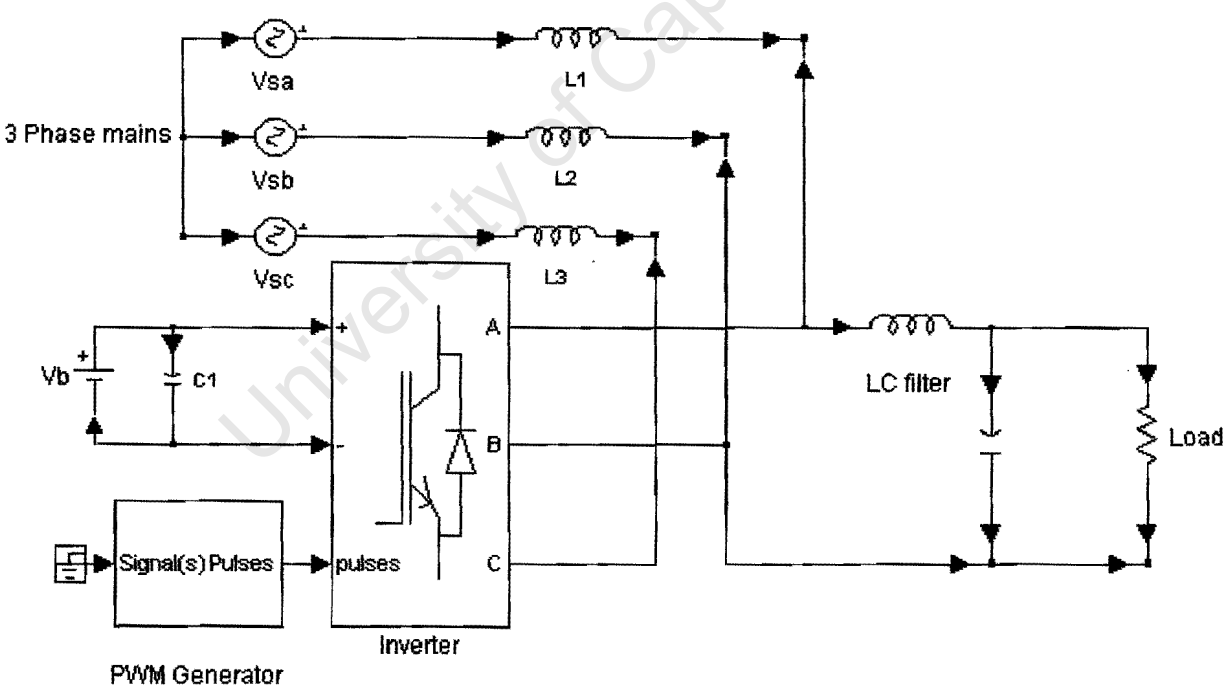

Figure 3-1: The proposed UPS Topology

When the mains fail, the UPS will be able to detect that the mains has failed. The utility supply is then isolated from the UPS through a static switch. Power goes on supplying the load uninterruptedly. Meanwhile the inverter converts battery power to ac power until the mains return or batteries are depleted.

The notable features of the proposed UPS topology are:

- The ability to draw balanced power from the utility and supplies it to a parallel combination of single loads.
- Phase lock the inverter output to the mains and use phase angle technique to charge batteries and regulate the dc bus. Phase angle technique is a method of controlling power flow through the link inductors by controlling both the magnitude and phase angle of the inverter output, relative to the incoming mains.
- Regulate the output voltage during both battery charging and battery discharging mode.
- Draw power at close to unity power factor from the utility.
- The ability to supply power to load uninterruptedly with no transfer time during power outage.

The schematic circuit diagram of the proposed component minimised UPS topology is illustrated in figure 3-1. The system is made up of three link inductors L1, L2, L3, battery pack represented on the circuit as Vb, three phase full bridge IGBT inverter and an LC filter.

Link Inductors

Three link inductors L1, L2 and L3 interface the three phase mains to the inverter. Link inductors act as buffers, they limit inrush currents from the mains and also filter out high order current harmonics.

Three Phase Full Bridge IGBT Inverter

The full bridge IGBT inverter has three pairs of IGBT switches shown on figure 3-1. Each pair controls a phase by operating the switches at high frequency in such a way that when top switch is on the bottom switch of the same pair is off. Space vector PWM pulses for switching the IGBTs are generated from a DSP board.

Battery Pack

The conventional lead acid batteries are used to form the DC bus. The batteries are charge in two phases, depending on the DC bus voltage. The bulk charge mode where a charging current is regulated at a specific current. Then the float voltage charge mode, which is a constant voltage charging.

LC Filter

An LC filter is used for filtering high switching frequencies (10kHz) leaving out the 50Hz fundamental frequency.

3.2 Basic Theory

The operating principles of the proposed UPS are based on Enjeti, Jae-Ho Choi and Feng approaches [10]. The operating principles are best explained with help of a simplified single-phase equivalent circuit illustrated in figure 3-2.

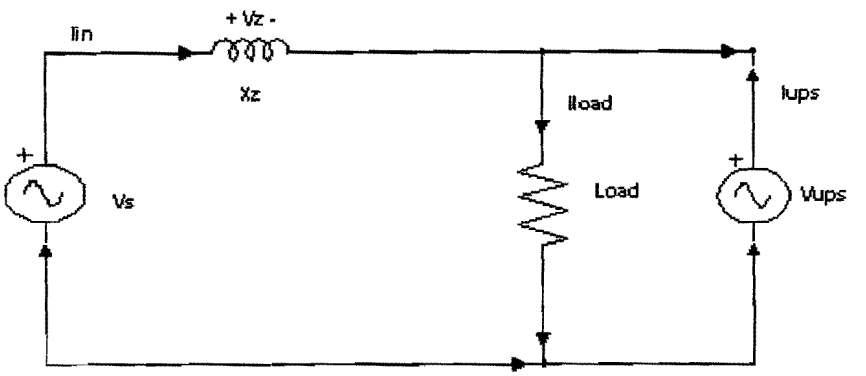

Figure 3-2: Simplified single phase equivalent circuit for the proposed UPS

On the circuit:

V_s is the mains supply voltage.

X_z is the link inductor

V_{ups} is the inverter output.

I_{ups} is the inverter output current.

I_s is the mains supply current.

I_{load} is the load current.

Applying Kirchoff's voltage and current laws in figure 3-2 the following equation can be derived:

$$V_s = V_{ups} + V_z \tag{3-1}$$

$$I_{load} = I_{ups} + I_s \tag{3-2}$$

$$I_s = \frac{V_z}{jX_z} \tag{3-3}$$

Where $X_z = \omega L_z$

Assuming the mains voltage to be a pure sine wave can be expressed as:

$$V_s(t) = V_s \sin(\omega t) \qquad (3\text{-}4)$$

The inverter output is assumed to be:

$$V_{ups}(t) = V_{ups} \sin(\omega t - \alpha) \qquad (3\text{-}5)$$

Assuming that the fundamental component of the load current I_{load} lags V_{ups} by β, then

$$I_{load}(t) = I_{load} \sin(\omega t - (\alpha + \beta)) \qquad (3\text{-}6)$$

From (3-4) and (3-5), the mains current can be obtained as:

$$I_s(t) = \frac{1}{\omega L_z} \int_0^t V_s \sin(\omega t) - V_{ups} \sin(\omega t - \alpha)) d(\omega t)$$

$$= I_s \sin(\omega t - \theta) \qquad (3\text{-}7)$$

The phasor diagrams of the above equations are shown in figure 3-3 and figure 3-5. The first phasor diagram is drawn with angle $\gamma = 90^o$. This would be the most likely situation. In the diagram the inverter voltage phasor V_{ups} lags the mains supply voltage phasor V_s by angle α and V_z is the voltage across the link inductor, represented by a phasor joining the inverter voltage V_{ups} to V_s.

The current through an inductor lags the voltage by 90 degrees, the current phasor I_s is drawn at 90 degrees to V_z. I_s lags V_s by an angle θ.

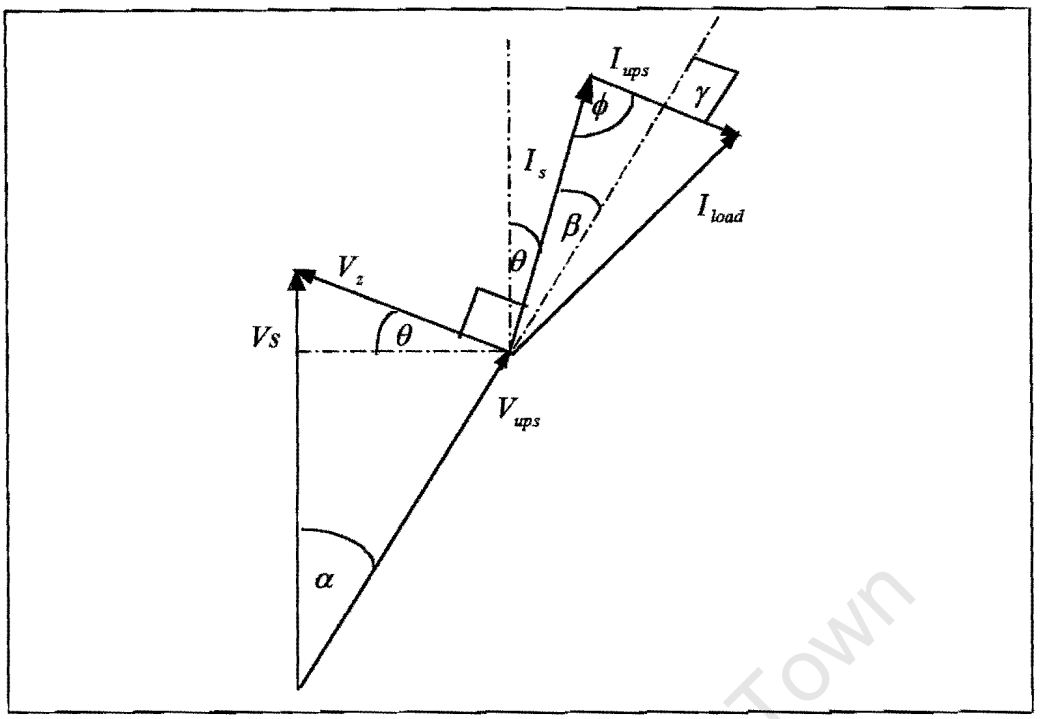

Figure 3-3 Phasor Diagram of singles Phase Equivalent Circuit, $\gamma = 90^o$

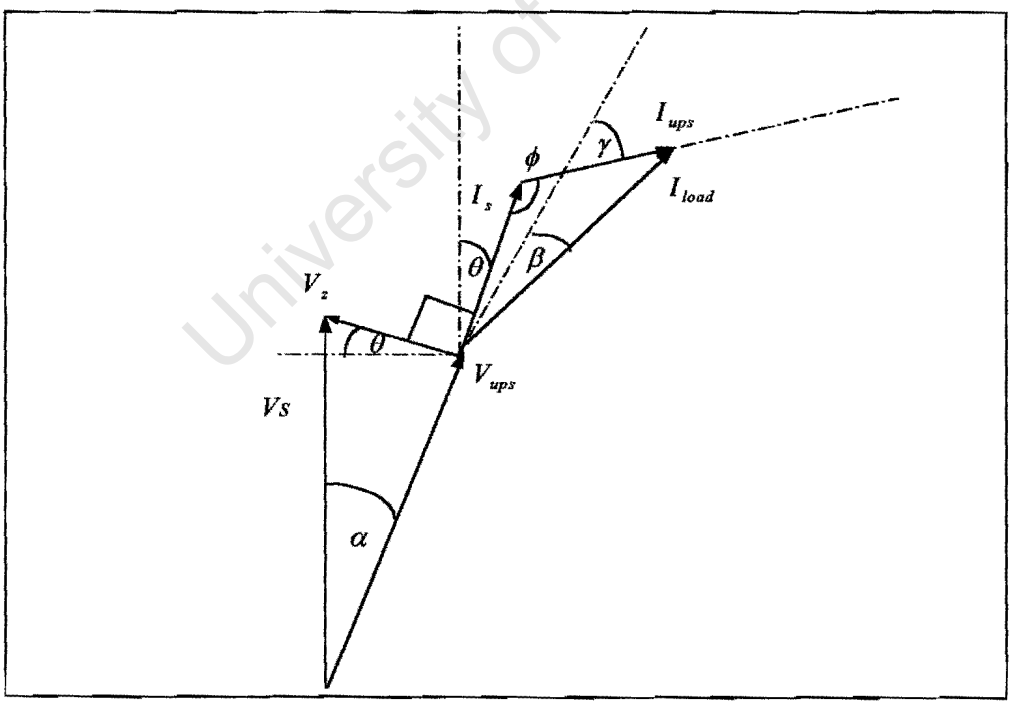

Figure 3-4: Phasor Diagram of singles Phase Equivalent Circuit, $\gamma = 40^o$

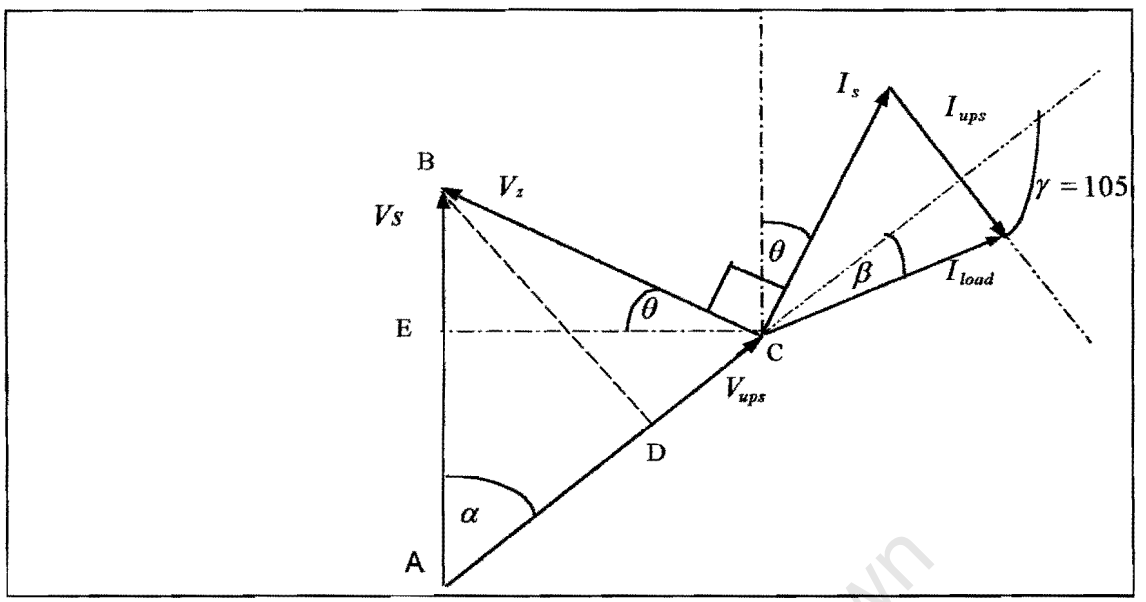

Figure 3-5: Phasor Diagram of singles Phase Equivalent Circuit, $\gamma = 105^o$

Note that when $\gamma > 90^o$ means that the UPS is charging batteries and when $\gamma < 90^o$ means the UPS is discharging batteries. When $\gamma = 90^o$ the UPS is absorbing zero power and the UPS spends the bulk of the time operating at this point.

The magnitude of the supply current I_s can be determined by trigonometry, considering triangle DBC.

$$I_s = \frac{V_z}{X_z} = \frac{1}{X_z}\sqrt{(V_{ups} - V_s\cos(\alpha))^2 + (V_s\sin(\alpha))^2} \qquad (3\text{-}8)$$

The angle θ can be given as:

$$\theta = \sin^{-1}\left(\frac{(V_s - V_{ups}\cos(\alpha))}{\sqrt{(V_{ups}\sin(\alpha))^2 + (V_{ups}\cos(\alpha) - V_s)^2}}\right) \qquad (3\text{-}9)$$

From figure 3-3 the phase angle γ between the UPS voltage V_{ups} and the inverter current I_{ups} is:

$$\gamma = 180^o - \phi + \theta - \alpha \qquad (3\text{-}10)$$

From equations (3-7) to (3-9), $I_{load}(t)$ and $I_s(t)$ are both sinusoidal signals. Note that $I_s(t)$ is independent of load current, and $I_{load}(t)$ is a pure sine wave because they are at the same node. The supply current is controlled by the phase angle α and by the size of the inductor X_z. The above relationship equations can be used to control power flow and input power factor.

3.3 Control Principles

There are two conditions of the mains during UPS operation:

- Mains outage condition and
- Mains ac normal operation

3.3.1 Mains Outage Condition

The converter only does a pure inverter function, discharging batteries. It yields regulated load voltage without considering the phase angle of the output voltage. But the output voltage phase angle is generated by the DSP in phase with the latest mains phase angle in its memory. The power flow in this condition excluding switching losses is given by:

$$P_{ups} = P_{load} \qquad (3\text{-}11)$$

3.3.2 Mains AC Normal Operation

The challenging part is how to control the converter voltage and phase angle α to ensure that the battery set is charged and the input power factor stays close to unit. In this operation mode there are two operating phases:

- The battery set charging phase
- The float voltage mode

Power through link inductors is controlled by varying the phase shift angle α. The relationship between the phase shift angle and power flow is derived from figure 3-4 using simple trigonometry as follows:

$$V_{ups}\sin(\alpha) = V_z\cos(\theta) \qquad (3\text{-}12)$$

Mains supply real power is given by:

$$P = V_s I_s \cos(\theta) \qquad (3\text{-}13)$$

Substituting for $\cos\theta$ from (11) we get:

$$P = \frac{V_s V_{ups}}{X_z}\sin(\alpha) \qquad (3\text{-}14)$$

The converter can operate bi-directionally, this is supported by the equation of real power flowing into the UPS bellow:

$$P_{ups} = V_{ups} I_{ups}\cos(\gamma) \qquad (3\text{-}15)$$

Where $\cos(\gamma)$ can be positive or negative value that determines the power flow. Phase angle α is used for controlling, making $0^o < \gamma < 180^o$. If the converter is lossless, the power going to or coming from the battery P_{bat} will equal P_{ups}.

The battery set-charging phase

The battery set-charging phase is a constant current I_{bat} charging phase. Power absorbed by the converter excluding losses is:

$$P_{ups} = P_{bat} = V_{bat} I_{bat} \tag{3-16}$$

The float voltage mode

The float voltage mode is a constant voltage-charging mode, where the dc bus V_{bat} is regulated at its maximum value by varying the phase angle α.

$$V_{bat} = \frac{P_{ups}}{I_{bat}} \tag{3-17}$$

3.4 Power Factor Correction

Input power factor is equal to $\cos\theta$ where θ is given by equation (3-9)

$$\cos(\theta) = \left(\frac{(V_s - V_{ups}\cos(\alpha))}{\sqrt{(V_{ups}\sin(\alpha))^2 + (V_{ups}\cos(\alpha) - V_s)^2}} \right) \tag{3-18}$$

Can also be expressed as:

$$\cos(\theta) = \frac{V_{ups}\sin(\alpha)}{\sqrt{(V_{ups} - V_s\cos(\alpha))^2 + (V_s\sin(\alpha))^2}} \tag{3-19}$$

Although the amplitude and phase of V_{ups} can be controlled to keep a unit power factor,

the UPS must maintain a specified load voltage. Therefore the amplitude of V_{ups} is controlled by the duty-ratio of PWM waveforms so as to keep a constant load voltage.

For a special case $\alpha = 0^o$, the angle θ of the input power factor becomes 90^o and consequently only reactive power flows, excluding losses. Which is a useless operation and should be avoided. Although with this UPS when ac mains is back after a power outage the UPS first phase locks ($\alpha = 0$) for about 30 seconds then the phase angle α is increased accordingly.

The UPS spends most of its operation time with $\gamma = 90^o$. At this pint the UPS is absorbing zero real power and operating at close unit power factor. When the supply voltage V_s changes the phase shift angle α is also changed so that a constant current I_s is supplied form the utility. The resulting value of the power factor calculated using equation 3-18 or 3-19, will be determined by the phase shift angle α and the new value of V_s, V_{ups} is kept constant all the time.

4 Space Vector Modulation

4.1 Introduction

Pulse Width Modulation (PWM) has been studied extensively during the past decade, with different PWM methods developed to achieve the following aims:

- Wide linear modulation range.
- Less switching loss.
- Less total harmonic distortion (THD) in the spectrum of switching waveform.
- Easy implementation and less computation time [6].

For a long period, carrier-based PWM methods were widely used in most applications. But with the development of microprocessors, space vector modulation has become one of the most important PWM methods for three-phase converters [7]. It is a digital implementation of the PWM modulators, using space vector concept to compute the duty circle of the switches. Elegant digital implementation is one of the notable features of space vector modulation and all the above benefits are achieved with this method.

4.2 Theory of SV PWM Technique

Space vector modulation is a method of analysing a three-phase system in terms of complex space vectors. The method transforms a three-phase stationary co-ordinate system to an orthogonal co-ordinate system.

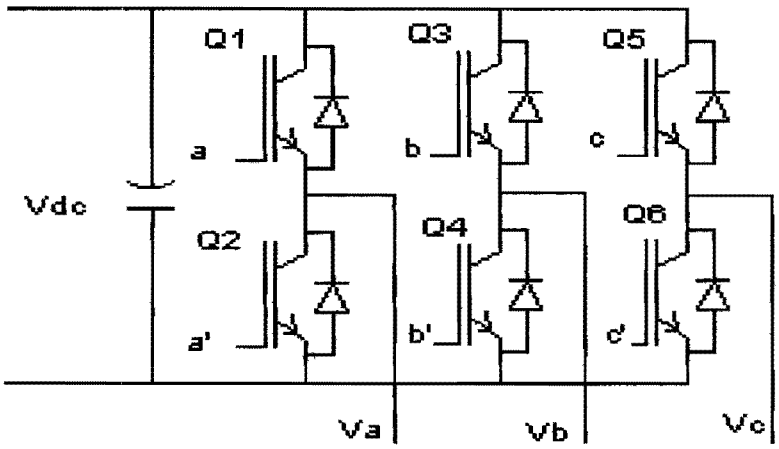

Figure 4-1: Three-Phase Two Level Voltage Source Inverter (VSI).

The structure of a three-phase two level VSI used for this project is illustrated in figure 4.1. Va, Vb and Vc are the line to neutral output voltages of the inverter. Power transistors Q1 through Q6 shape the output voltages [8]. The Power transistors are controlled by a, a', b, b' c, and c'. When upper transistor is switched on (1) the corresponding lower transistor is off (0).

The relationship between the switching variable vector [a, b, c] and the line to line output voltage vector [Vab, Vbc, Vca] is given by the following equations.

$$Vab = (a - b) * Vdc \tag{4.1}$$

$$Vbc = (b - c) * Vdc \tag{4.2}$$

$$Vca = (c - a) * Vdc \tag{4.3}$$

There are eight possible combinations of the on (1) and off (0) states for Q1, Q3 and Q5. The vector representation of the phase voltages corresponding to the eight combinations can be obtained by applying the so-called d-q transformation to the phase voltages. A d-q transformation is an orthogonal projection of [a, b, c] onto a two dimensional plan

perpendicular to vector [1, 1, 1] in a three dimensional co-ordinate system. The d-q transformation equation is given bellow.

$$\begin{bmatrix} Vd \\ Vq \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{\frac{3}{4}} & -\sqrt{\frac{3}{4}} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{4.4}$$

The results are six non-zero vectors and two zero vectors. The nonzero vectors form the axes of a hexagon, illustrated in figure 4-2. The eight vectors called the basic space vectors are U0, U1, U2, U3, U4, U5, U6 and U7. The d-q transformation can be applied to desired three-phase voltage output to obtain a desired reference voltage U*out* in the d-q plane.

The objective of the SV PWM technique is to approximate the reference voltage U*out* instantaneously by combination of switching states corresponding to the basic space vectors.

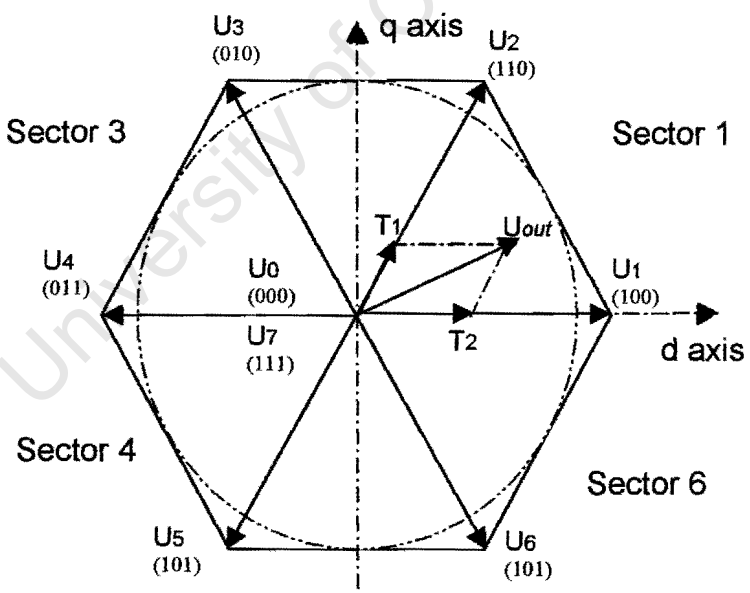

Figure 4-2: The Basic Space Vectors

T1 and T2 are the respective duration of which switch states U1 and U2 are applied (the basic space vectors that form sector containing U*out*) For small period time T change in

reference voltage U_{out} is tiny.

In the vector space the following rules are obeyed according to the equivalence principle.

$$\overrightarrow{U1} = -\overrightarrow{U4}$$
$$\overrightarrow{U2} = -\overrightarrow{U5}$$
$$\overrightarrow{U3} = -\overrightarrow{U6}$$
$$\overrightarrow{U0} = -\overrightarrow{U7} = \vec{0}$$
$$\overrightarrow{U1} + \overrightarrow{U3} + \overrightarrow{U5} = \vec{0}$$

In one sampling interval, the output voltage vector U_{out} can be written as:

$$\overrightarrow{U(t)} = \frac{t0}{T}\vec{U}0 + \frac{t1}{T}\vec{U}1 + \ldots + \frac{t7}{T}\vec{U}7 \qquad (4.5)$$

Where t0, t1...t7 are the turn on time of the vectors U1...U7.

$t0, t1, ..t7 \geq 0, \sum_{i=o}^{7} ti = T$ and T is the sampling time.

According to (4.5) the decomposition of $\vec{U}$ into $\overrightarrow{U1}, \overrightarrow{U2}, ..\overrightarrow{U7}$ has infinite ways. In order reduce the number of switching actions and making full use of active turn on time for space vectors the vector $\vec{U}$ is split into the two nearest adjacent voltage vectors and zero vectors $\overrightarrow{U0}$ and $\overrightarrow{U7}$ in an arbitrary sector.

In sector one, in one sampling time interval T, vector $\vec{U}$ can be expressed as:

$$\vec{U} = \frac{T1}{T}\overrightarrow{U1} + \frac{T2}{T}\overrightarrow{U2} + \frac{T7}{T}\overrightarrow{U7} + \frac{T0}{T}\overrightarrow{U0} \qquad (4.6)$$

Where: $T - T1 - T2 = T0 + T7 \geq 0, T0 \geq 0, T7 \geq 0$

In linear modulation range the trajectory of $\vec{U}$ is the inscribed circle of the hexagon and the maximum amplitude of the sinusoidal line to line voltage is the dc-bus voltage.

Therefore the phase voltage is given by $\frac{Vdc}{\sqrt{3}}$ (4.7)

And Maximum modulation amplitude $M_{\max} = \frac{Vdc}{\sqrt{3}} * \frac{2}{Vdc} = 1.15$ (4.8)

$M_{\max}$ is 15% more than the conventional sinusoidal PWM.

4.3 Space Vector Modulation Algorithm

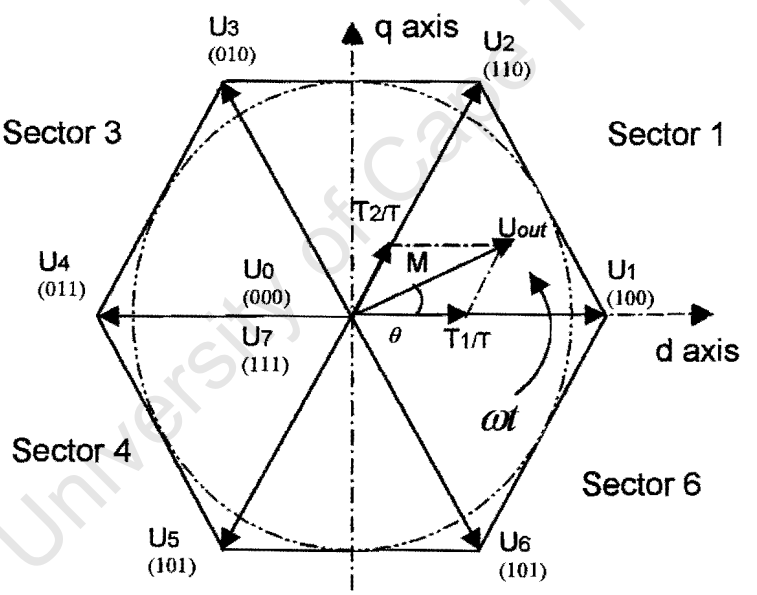

Figure 4-3: Modulation range

Late the length of $\overrightarrow{Uout}$ be M, illustrated in figure 4-3 above.

Looking at triangle with sides T1/T, T2/T, M and angle the θ, applying sine rule:

$$\frac{M}{\sin\frac{2\pi}{3}} = \frac{T1}{T}\frac{1}{\sin(\frac{\pi}{3}-\theta)} = \frac{T2}{T1}\frac{1}{\sin\theta}$$

Thus,

$$\frac{T1}{T} = \frac{2}{\sqrt{3}}M\sin(\frac{\pi}{3}-\omega t) = \frac{2}{\sqrt{3}}M\cos(\omega t+\frac{\pi}{6}) \quad (4.9)$$

$$\frac{T2}{T} = \frac{2}{\sqrt{3}}M\sin(\omega t) = \frac{2}{\sqrt{3}}M\cos(\omega t+\frac{3\pi}{2}) \quad (4.10)$$

T0 + T7 = T –T1 –T2

Where $2n\pi \le \omega t = \theta \le 2n\pi + \frac{\pi}{3}$

The basic vectors and the zero vectors determine the length and angle of Uout. The decomposition of U_{out} in all six sectors is shown in Table 1. Different distribution of T0 and T7 for zero vectors yields different space vector PWM modulators. There are no separate modulation signals in each of the three phases in space-vector modulation technique [11]. Instead, a voltage vector is processed as a whole [7].

Table 3.1 Space Vector Algorithm

Sector	Algorithm	
1 $(0 \le \omega t \le \frac{\pi}{3})$	$T1 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{\pi}{6})$ $T2 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{3\pi}{2})$	$T0 + T7 = T - T1 - T2$
2 $(\frac{\pi}{3} \le \omega t \le \frac{2\pi}{3})$	$T2 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{11\pi}{6})$ $T3 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{7\pi}{6})$	$T0 + T7 = T - T2 - T3$
3 $(\frac{2\pi}{3} \le \omega t \le \pi)$	$T3 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{3\pi}{2})$ $T4 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{5\pi}{6})$	$T0 + T7 = T - T3 - T4$
4 $(\pi \le \omega t \le \frac{4\pi}{3})$	$T4 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{7\pi}{6})$ $T5 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{\pi}{2})$	$T0 + T7 = T - T4 - T5$
5 $(\frac{4\pi}{3} \le \omega t \le \frac{5\pi}{3})$	$T5 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{5\pi}{6})$ $T6 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{\pi}{6})$	$T0 + T7 = T - T4 - T5$
6 $(\frac{5\pi}{3} \le \omega t \le 2\pi)$	$T6 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{\pi}{2})$ $T1 = \frac{\sqrt{3}}{2} MT \cos(\omega t + \frac{11\pi}{6})$	$T0 + T7 = T - T1 - T6$

5 Proposed Topology Simulations

5.1 Introduction

Simulations were done with an aim to learn, analyse and apply practically the theory of the proposed UPS topology. Matlab simulations and mathematical simulations were carried out on a single-phase model to investigate the effects of different variables. When a compromised solution on the variable was found, matlab simulations were then carried out on a three-phase model.

Mathematical simulation method was developed using mathematical equations derived from phasor diagrams in chapter three. Using the mathematical simulation method, relationships between variables could be easily investigated. The investigations were carried out to provide insight into the control strategy for the UPS. To find a suitable compromise solution for each variable, and to ensure that all the objectives of the project were achieved. Variables that were investigated illustrated in figure 5-1 are:
Phase angle α, supply current I_s, UPS current I_{ups}, and also supply power, UPS power, supply power factor and UPS power factor.

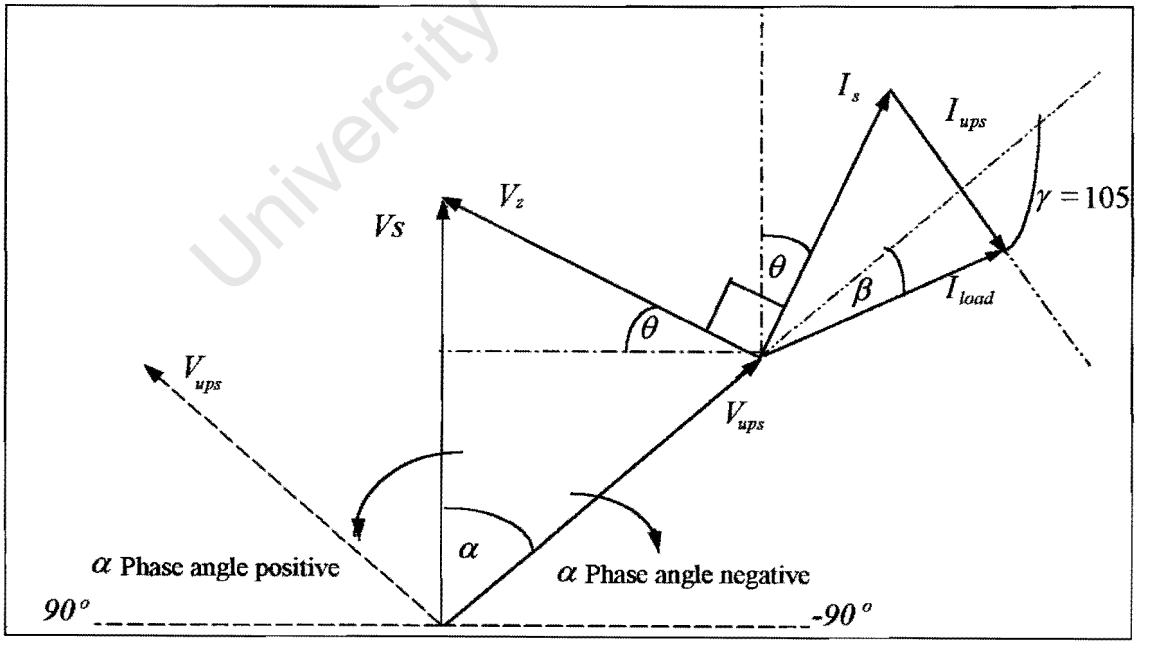

Figure 5-1: Phase Angle Range α

5.2 Matlab Simulations of a Single Phase UPS Model

The single-phase equivalent circuit of the proposed UPS model shown bellow was simulated. The UPS model with all the measurement tools used for simulation is shown in Appendix A.

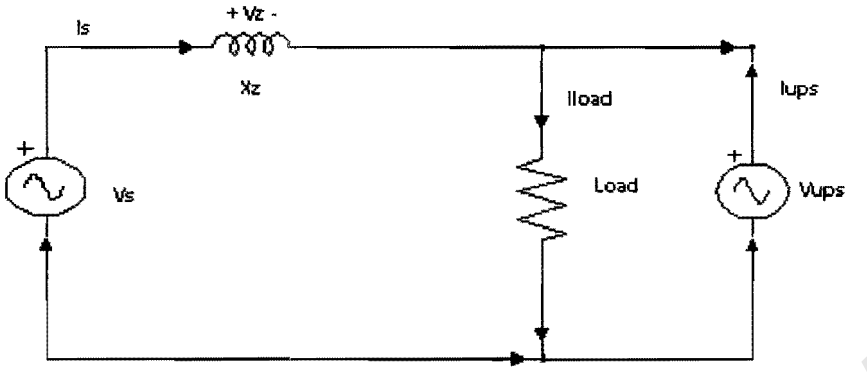

Figure 5-2: The Simulated single-phase model of the proposed UPS

The main idea of this project is to control power flow through the link inductor by controlling the phase angle α. From equation one from chapter three:

$$P = \frac{V_s V_{ups}}{X_z} \sin(\alpha) \qquad (5.1)$$

it can be seen that the supply power is directly proportional to the sine of phase angle α but inversely proportional to inductor X_z with a constant of proportionality $V_s V_{ups}$.

Simulations were done with an aim of selecting the best range for phase angle α and selecting the best inductor size X_z. Bearing in mind that supply power factor should stay close to unit all the time during operation of the UPS.

5.2.1 Supply Current Flow

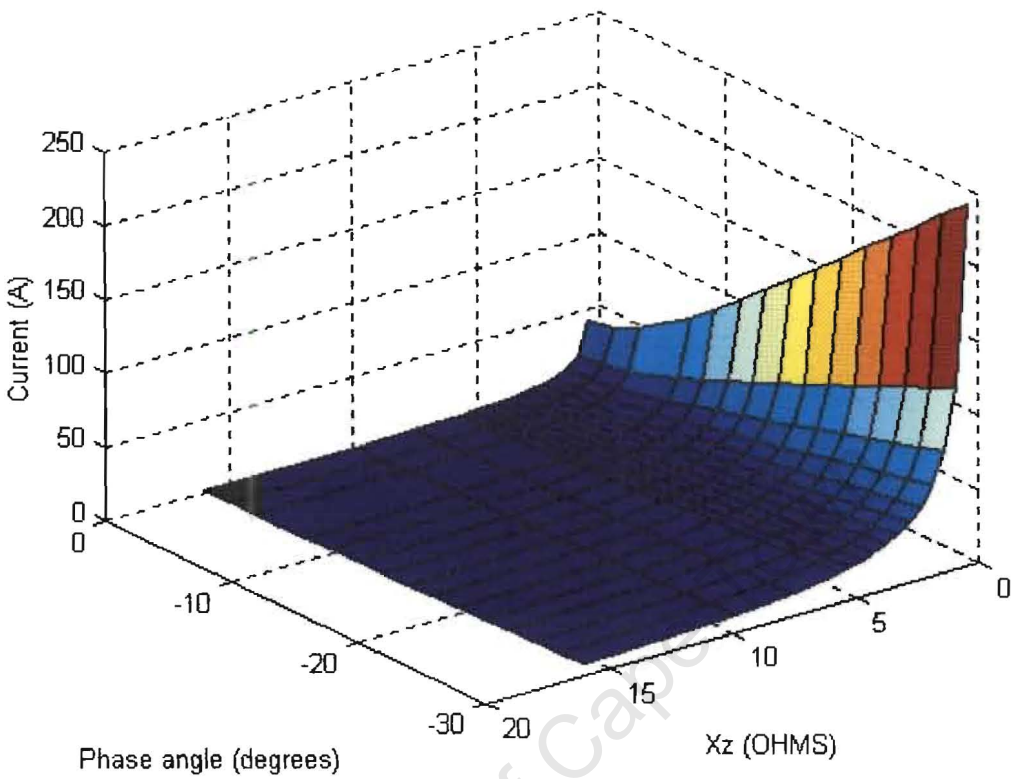

Figure 5-3: The Effects of changing Phase Angle and Link Inductance simultaneously on Supply Current

Figure 5-3 shows the effects that the phase angle and link inductance has on the supply current. The phase angle was varied between 0 to 30 degrees whilst the link impedance was varied between 0.47 and 16 ohms. The supply voltage and the UPS voltage were kept constant.

It can be seen that the current increases with an increase in phase angle α and decreases with an increase in link inductance.

Note that if $V_s = V_{ups}$ then $V_z = 2\sin(\alpha/2)$, this illustrated on figure 5-4.

The current that flows is given by:

$$I_s = \frac{2V_s \sin(\alpha/2)}{X_z} \qquad (5.2)$$

Therefore I_s is proportional to $\sin(\alpha/2)$ and inversely proportional to link inductance.

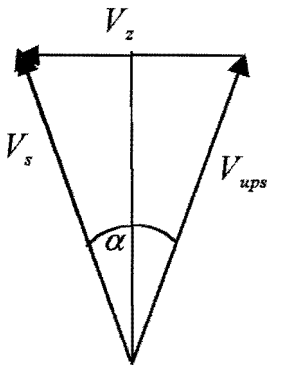

Figure 5-4: Phasor diagram when $V_s = V_{ups}$

This means that the smaller the inductor is, the more current will flow through it per small change in phase angle making it more difficult to control the flow of power when the inductor is small. A big inductor would mean easier control of power from the supply to the UPS and also better buffering by the inductor, but less power will be supplied to the UPS per given charge in phase angle.

Therefore a compromised solution was needed for phase angle range and size of the inductor to give a stable system and provide the required power to the load at close to unit power factor.

5.2.2 The effects of changing Phase Angle α

All the simulations in this section were carried out with a constant resistive load under the following conditions:

Load Power = 7.5 kW

Supply Voltage V_s = 220V

UPS Voltage V_{ups} = 230V

Load current I_{load} = 32.6A

Inductor X_z = 4.5Ω

Phase angle α was changed in steps of 2 degrees from -90^o to 90^o. When phase angle α is negative, V_{ups} is lagging V_s and power flows from the supply to the UPS. For this project the possible range for α is from -90^o to 0^o only allowing power to be drawn from the mains utility.

From 0^o to 90^o, V_{ups} is leading V_s and power is flowing from the UPS to the mains utility. Therefore power from the batteries or any dc supply is supplied to the grid. This shows that by phase angle control, power can be controlled to flow from the mains utility to the dc side of the inverter or vice versa.

The effects of changing phase angle α on Supply Power PF and UPS PF

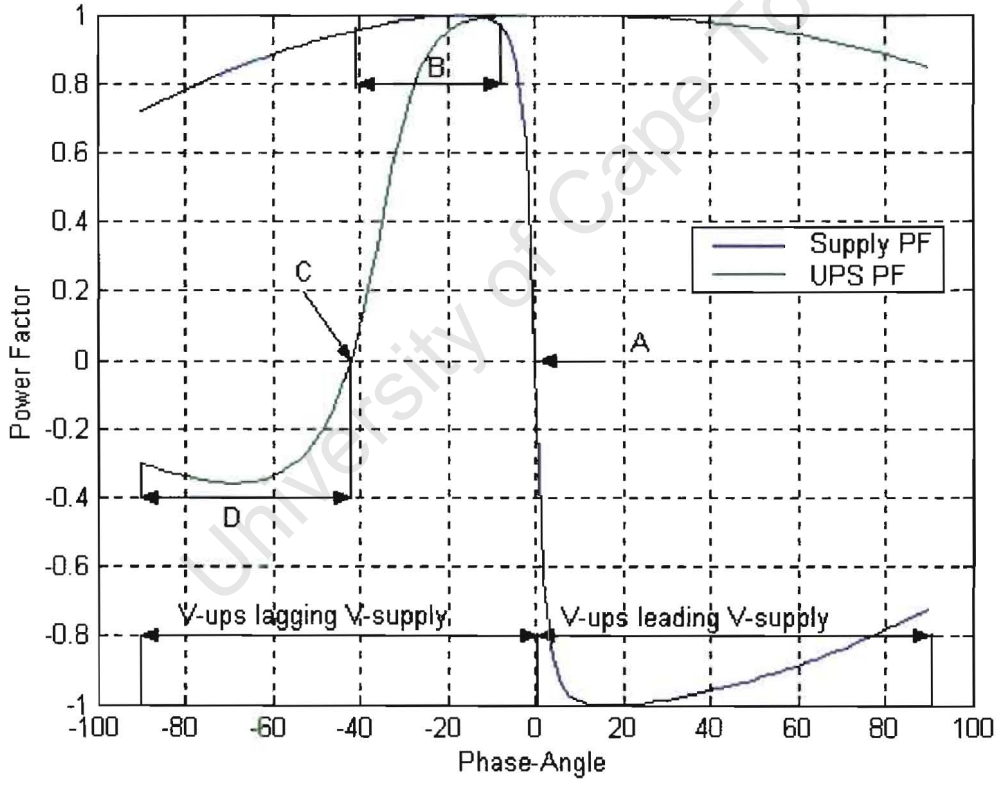

Figure 5-5: The effects of changing phase angle α on Supply Power PF and UPS PF

Figure 5-5 shows two graphs, supply power factor (PF) and UPS PF plotted against phase angle. The supply PF is the cosine of the angle between V_s and I_s, angle θ. The

UPS power factor is the cosine of the angle between V_{ups} and I_{ups}, angle γ. The angles are illustrated in figure 5-1. When γ is greater than 90 degrees the PF becomes negative and the UPS will be absorbing power.

Point A on the graph is a special case when phase angle α = 0, V_{ups} will be phase locked to supply voltage V_s. At this point, during the operation of the UPS a static switch is switched on connecting V_{ups} to V_s. This is only done when V_s is within the acceptable value. The UPS operate at this point for a few seconds allowing the system to stabilise after switching on the static switch. During this time the angle θ becomes 90 degrees consequently only reactive power flows from the supply. Therefore phase locking time should not be too long.

The UPS acceptable power factor range is labelled B on the graph. The acceptable PF range is when the PF is greater than 0.92.

Point C shown above is very important, I_{ups} is at 90^o to V_{ups}, which means that only reactive power flows to the UPS. The UPS does not consume real power at this point. This means that the load consumes all the supply power. No power is supplied to the batteries. This is the point where the UPS spends most of its operating time, and the voltage regulation point. The challenge is to operate the point C within the acceptable PF range B.

When α is in the range C, angle $\gamma > 90^o$ and its cosine negative which means that the UPS is absorbing power. This is the battery charging range.

The effects of changing phase angle α on I_s and I_{ups}

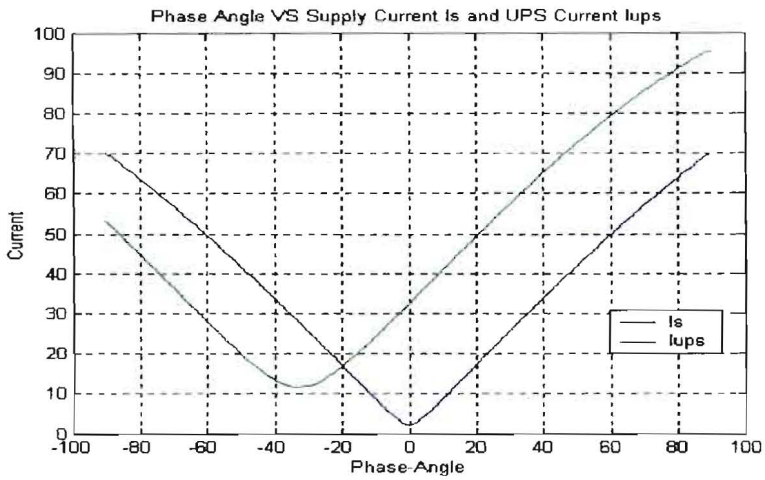

Figure 5-6: The effects of changing phase angle α on I_s and I_{ups}

From figure 5-6 it can be seen that the current from the supply and the UPS increases with the increase in phase angle. The ratio I_s to I_{ups} depends on the position of the phase angel and I_s never goes to zero. Unit power factor is achieved when I_s is equal to I_{ups}. When phase angle is zero, current to the load is supplied by the UPS.

The effects of changing phase angle α on Supply Power

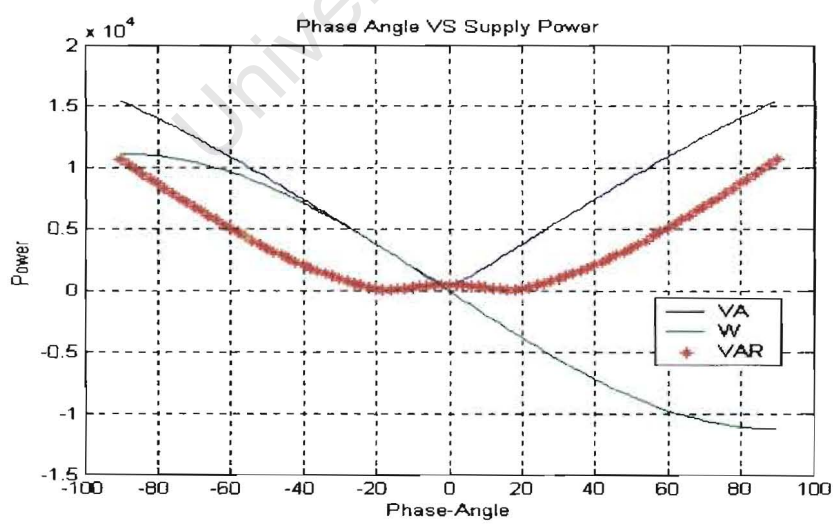

Figure 5-7: The effects of changing phase angle α on Supply Power

Figure 5-7 shows plot of apparent power, real power and reactive power from the supply as the phase angle is changed. Power is positive when the utility is supplying power to the load and UPS, and its negative when the mains utility is absorbing power. The PF is unity when apparent power is equal to real power. In the graph reactive power is never negative, it is calculated as:

$$P_{VAR} = \sqrt{P_{VA}{}^2 - P_W{}^2}$$

$$= P_{VA}\sqrt{(1-(PF)^2} \qquad (5.3)$$

Where:

P_{VAR} is the supply reactive power

P_{VA} is the supply apparent power

$P_W = P_{VA}\cos\theta$ is the supply real power and

$PF = \cos\theta$ is the supply power factor

The reactive power graph is supposed to be negative between phase angle of -20 and 20 degrees.

The effects of changing phase angle α on UPS Power

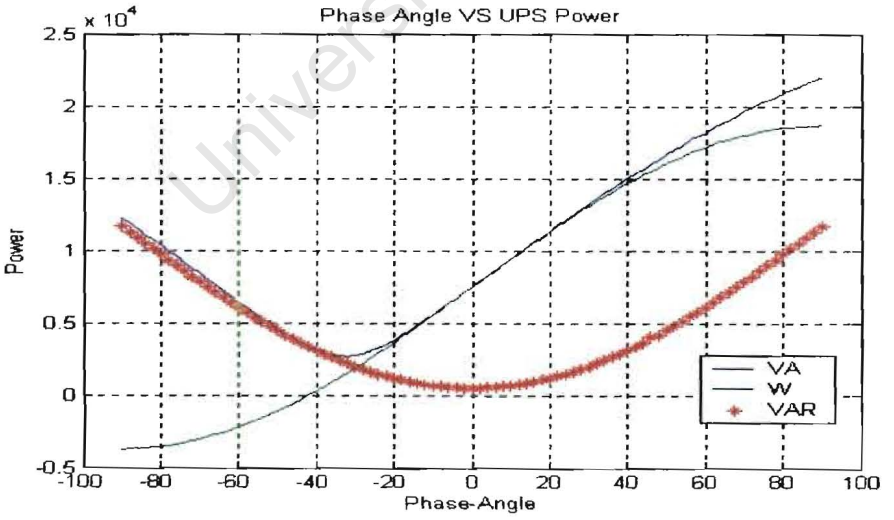

Figure 5-8: The effects of changing phase angle α on UPS Power

The graph of phase angle VS UPS shows that it's possible for the UPS to absorb zero real power by controlling the phase angle. The UPS is absorbing power for battery charging in the region where real power is negative.

5.2.3 The Effects of changing the link impedance X_z

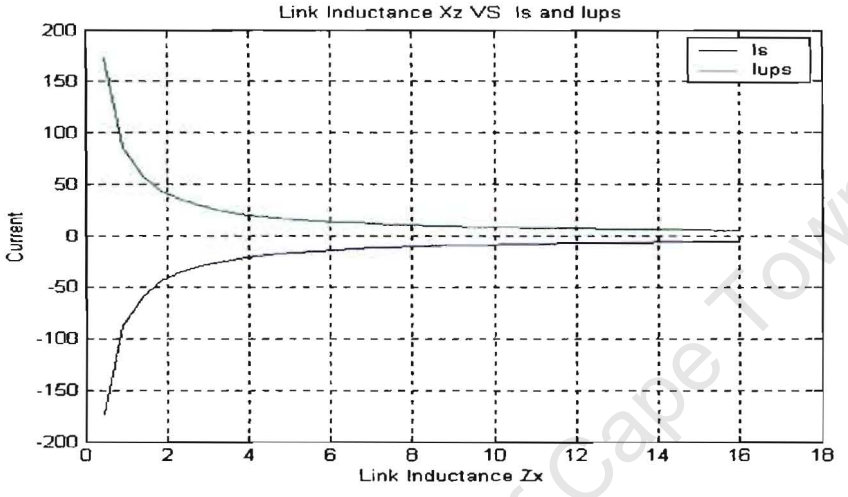

Figure 5-9: The Effects of changing the link impedance on I_s and I_{ups}

The effects of changing link impedance were carried out with a constant phase angle of 30 degrees and changing link inductance from 1.5mH to 51mH at 50Hz frequency. The plot of the results, figure 5-9, I_s and I_{ups} decrease exponentially with the increase in link impedance at the beginning, then rate of decrease of the current became smaller and smaller as the link impedance was increased. Similar graphs were produced for the supply power and UPS power flow. Changing the link impedance had no effect on the supply PF.

5.3 Mathematical simulations

Mathematical equations derived from phasor diagrams illustrated in chapter four where used to develop a simulating method. The following equations were used in developing the simulation method. See figure 5-1 for the labelling of voltages, currents and angles.

$$V_z = \sqrt{(V_{ups} - V_s \cos(\alpha))^2 + (V_s \sin(\alpha))^2} \quad (5.4)$$

$$I_s = \frac{V_z}{X_z} = \frac{1}{X_z}\sqrt{(V_{ups} - V_s \cos(\alpha))^2 + (V_s \sin(\alpha))^2} \quad (5.5)$$

$$I_{ups} = \sqrt{I_s^{\,2} + I_{load}^{\,2} - 2 * I_s * I_{load} * \cos(\alpha + \beta - \theta)} \quad (5.6)$$

$$\theta = \sin^{-1}\left(\frac{(V_s - V_{ups}\cos(\alpha))}{\sqrt{(V_{ups}\sin(\alpha))^2 + (V_{ups}\cos(\alpha) - V_s)^2}}\right) \quad (5.7)$$

$$\gamma = 180^o - \phi + \theta - \alpha \quad (5.8)$$

θ is the angle between V_s and I_s, cosine θ gives the supply power factor (PF). γ is the angle between V_{ups} and I_{ups}, cosine of γ gives the UPS PF. If the load is reactive the fundamental component of the load current I_{load} would lag V_{ups} by an angle β, illustrated in figure 5-1.

Simulations on the effects of changing phase angle α from –90 to 90 degrees was carried out under the same conditions as the simulations in simulink. The results from the mathematical simulations plotted graphs identical to the graphs obtained from simulink.

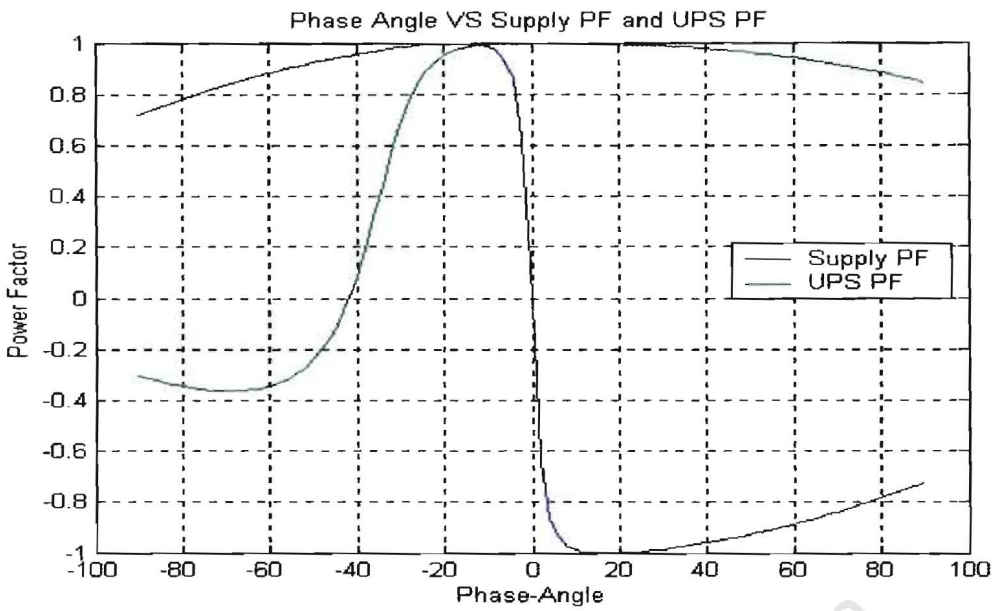

Figure 5-10: The effects of changing phase angle α on Supply Power PF and UPS PF using mathematical simulations.

Figure 5-10 shows the effects of changing phase angle on Supply PF and UPS PF using mathematical simulations. The graph is identical to the graph obtained using simulink figure 5-5, simulated under same conditions. Since mathematical simulations were identical to simulink simulations and can be easily manipulated to shows effects α and X_z on power flow. Mathematical simulations were used to obtain the graphs that follow.

5.3.1 Power flow when $V_s = V_{ups}$

The simulations below were carried out with a resistive load and the following:

Load Power = 7.5 kW

Supply Voltage V_s = UPS Voltage V_{ups} = 230V

Load current I_{load} = 32.6A

Angle $\beta = 0$

Inductor X_z = 4.5 Ω

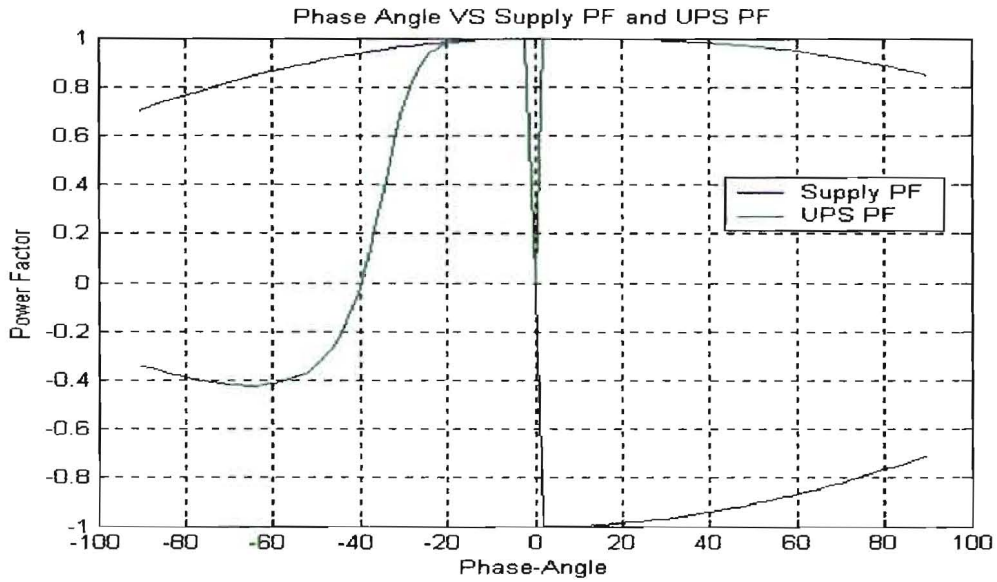

Figure 5-11: Power flow when $V_s = V_{ups}$

When $V_s = V_{ups}$, The acceptable PF is achieved within the range –2<α<-20 degrees and battery charging only starts when α<-40. See figure 5-10 above.

5.3.2 Power flow when V_s is 10 percent greater than V_{ups}

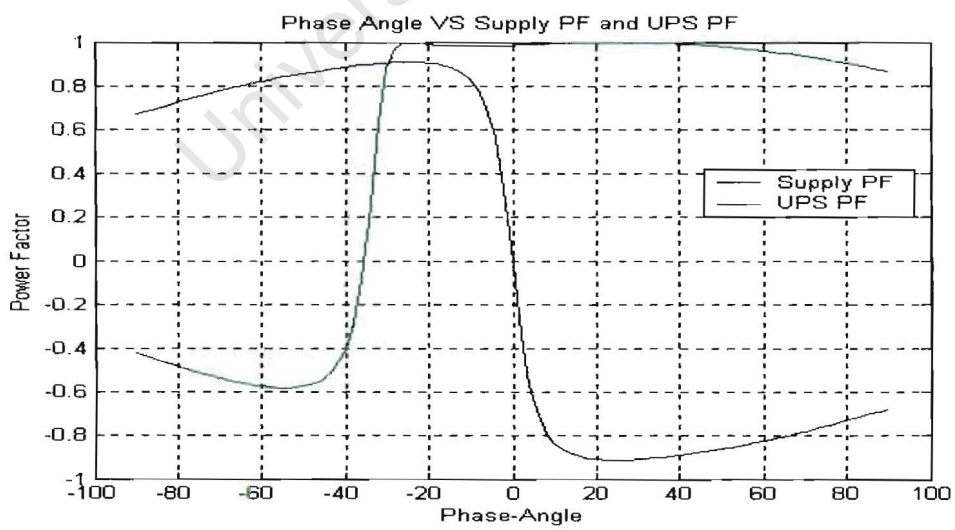

Figure 5-12: Power flow when V_s 10 percent greater than V_{ups}

Figure 5-12, V_s is 10 percent greater than V_{ups} the acceptable PF can not be achieved the maximum PF factor is 0.9. Battery charging only starts when α <-34 degrees.

5.3.3 Power flow when V_s is 10 percent less than V_{ups}

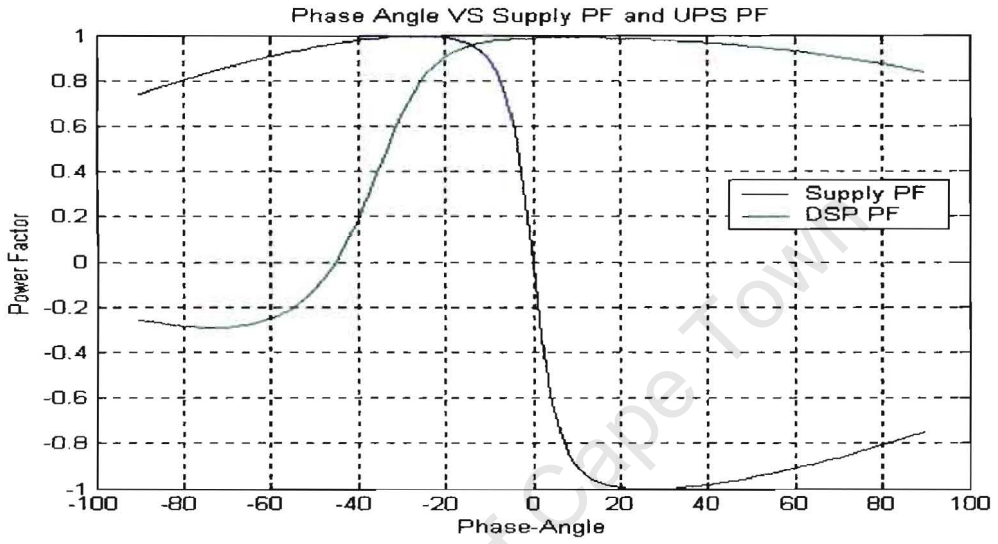

Figure 5-13: Power flow when V_s is 10 percent less than V_{ups}

In figure 5-13 V_s is 10 percent less than V_{ups}. The acceptable PF range is achieved in the range –18<α <-38 degrees. UPS absorbs power when α <-46 degrees.

5.3.4 Effects of angle β on UPS power flow

If the load in reactive the fundamental component of the load current I_{load} would lag V_{ups} by an angle β, illustrated in figure 5.1. Charging angle β from zero to about 45 degrees had no effect on the supply PF, but shifts the angle by a few degrees at which the UPS starts to absorb power to the left or to the right depending on the size of β.

5.3.5 Power flow of a 230V, 5kW UPS System

The central idea is to control flow of power through the link inductor by controlling phase angle α, regulating the dc bus without the inverter consuming real power from the supply. And also to enable battery charging when necessary. The UPS operating at unit PF all the time.

By careful selection of maximum load power and link inductor size all the desired objectives of the project can be achieved. The simulations below show results of the system carried out with the following values:

Load Power = 5 kW

Supply Voltage V_s = UPS Voltage V_{ups} = 230V

Load current I_{load} = 21.7A (pure resistive), angle $\beta = 0$

Inductor X_z = 2.5Ω

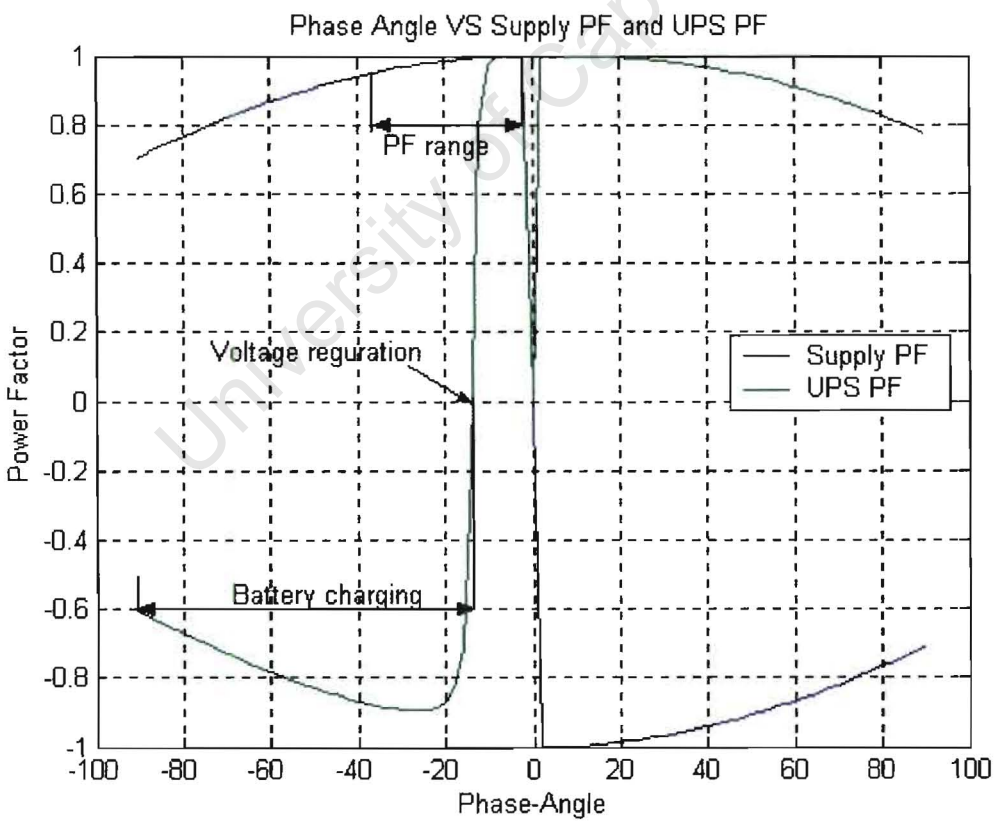

Figure 5-14: Power flow of a 230V, 5kw UPS System

Figure 5-14 shows the power flow of the intended UPS system that would be connected directly to three-phase mains supply.

Voltage regulation

The UPS regulate voltage at the point illustrated in figure 5-14. At this point the UPS would be operating within the acceptable power factor range. During voltage regulation it should be noted that I_s is controlled by shifting of phase angle α, going to the right of the voltage regulation point would increase I_s, and going to the left would decrease I_s. V_{ups} is controlled by the duty ration of the PWM waveforms. Since the system has no control of the supply voltage, when supply voltage decreases, phase shift angle is increased making the mains supply constant current. When the supply voltage is 10% lower than V_{ups}, the system can be made to operate in the acceptable PF factor range as in figure 5-12. So by using a combination of the phase angle control and duty ration of PWM waveforms the mains can be made to supply constant current, and operating within the acceptable power factor range all the time. When V_s is less than 50% of V_{ups} the supply voltage is isolated from UPS using a static switch and power to the load is supplied by the UPS.

Battery Charging

The battery charging range is $-90 < \alpha < -12$ degrees. In this range phase angle control is used to control the amount of power absorb by the UPS for battery charging. A certain maximum battery charging current of is maintained. As the battery set charges up phase angle is gradually reduced causing battery power and battery current to also become smaller. When the battery set is fully charge then I_{ups} would be at 90^o to V_{ups} and UPS power absorbed would be zero. During this battery charging operation the UPS maintains V_{ups} at 230V by controlling the duty ratio of PWM waveforms. In this operating mode, priority is given to battery recharging. Batteries are charged as quickly as possible

without considering power factor value.

5.4 Laboratory Prototype UPS

The Laboratory prototype UPS was simulated with a resistive load and the following:

Load Power = 2.5 kW

Supply Voltage V_s = UPS Voltage V_{ups} = 100V

Load current I_{load} = 15 A (pure)

Angle $\beta = 0$

Inductor X_z = 1.7 Ω

Figure 5-14 shows the power flow of the laboratory prototype UPS. V_{ups} was regulated at 100V phase angle at –10 degrees with V_s at 100V.

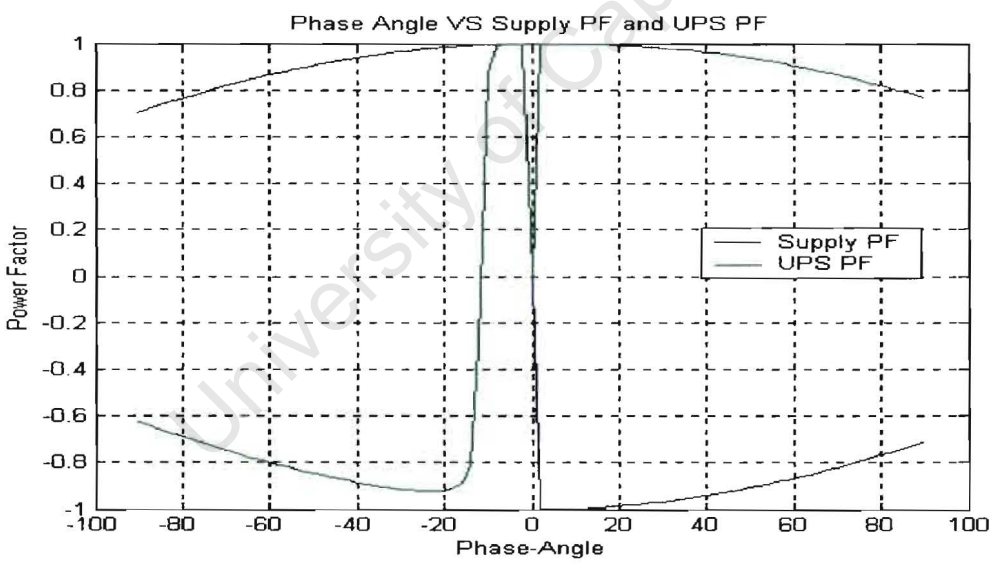

Figure 5-15: Power Flow of the Laboratory Prototype UPS

5.5 Matlab Simulations of Three Phase UPS Model

Three phase simulations were carried out with an aim to applying the single operating principal to a three-phase system, to understand phase locking and voltage regulation of the UPS topology. The three-phase UPS model and simulations are shown in Appendix A.

6 Hardware Description

6.1 Introduction

Following is a description of the hardware used for building three-phase to single-phase UPS laboratory prototype. A UCT developed board based on the Texas Instrument TMS320F243 Digital Signal Processor (DSP) was used for control applications. The reasons for choosing this DSP board are stated below. A brief description of 243_DSP board and the compiler software is given in this section. This document focuses on the main functions of the 243_DSP-development board that were used for this project. For detailed information on the TMS320F243 DSP please see Appendix B.

6.2 Choosing a controller for UPS

Today's low-cost, high-performance Texas Instrument TMS320F243 DSP controller provides an improved and cost effective solution for the UPS design. The DSP has integrated peripherals specifically chosen for embedded control applications. These include the event manager module, which provides general –purpose timers and PWM registers to generate PWM outputs, and 10-bit analog-to-digital converters (ADCs).

High CPU bandwidth and the integrated power electronic peripherals make it possible to implement a complete digital control of the UPS design. Multiple control algorithms can be executed at high speed enabling high sampling rate for good dynamic response [14].

Digital control has the following advantages:

- Programmability, easy to update systems with enhanced algorithms for improved reliability.
- Immunity to noise
- Eliminates redundant voltage and current sensors for each controller.
- System has few components; less engineering time and system can be made smaller and reliable.
- DSP can communicate to host systems and I/O devices such as LCD displays. [14]

6.3 TMS320F243 DSP Key Features

The TMS320F243 DSP board is illustrated in figure 6-1. The major features of the board are listed bellow.

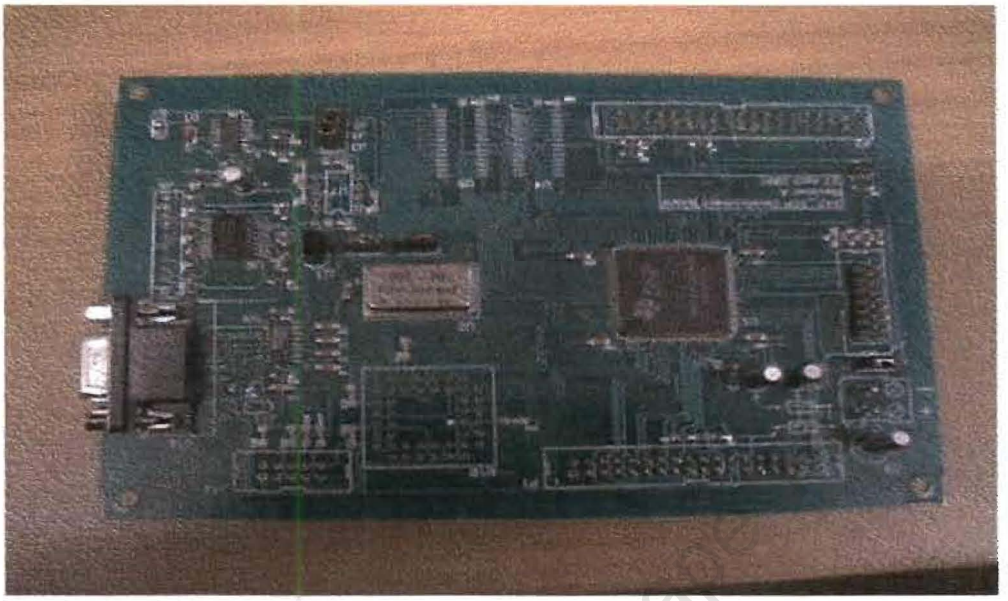

Figure 6-1 TMS320F243 DSP board

- A 16 bit fixed point DSP running at 20MHz giving the CPU core 50ns instruction cycle time.
- Internal memory modules are dual access random-access memory (DARAM) and Flash memory. There are 544 words x 16 bits of DARAM. DARAM allows writes and reads from the RAM in the same cycle. Flash EEPROM has advantage of reprogrammability. It incorporates one 8k x 16 bit flash EEPROM module in program space.
- Two general-purpose (PG) timers which can be operated independently or synchronised with each other. Each timer has a 16 bit compare unit capable of generating one independent PWM output. There are three continuous modes of operation of each GP timer in up - or up/down-counting operations.
- Three full-compare units using GP timer one as time base and generating six outputs for compare and PWM waveform using programmable dead-band circuit.

- 10-bit ADC with a built in sample and hold (S/H) circuit. There are eight analog input channels. Maximum conversion time for each ADC unit is 1 μ s. Reference voltage for the ADC module is 0 - 5V and is supplied externally.
- Watchdog (WD) timer module monitors software and hardware operation. It generates a system reset if it is not periodically serviced by software by having the correct key written. WD timer operates independently of the CPU and always enabled.
- 32 general-purpose, bi-directional digital I/O (GPIO) pins. Six are dedicated I/O pins and 26 pins are shared between primary function and I/O.
- CPU support one non-maskable interrupts (NMI) and six maskable prioritised interrupts request. The device has many peripherals and each peripheral is capable of generating one or more interrupts in respond to many events.
- Power drive protection (PDPINT) input for safe operation of the power converter.
- RS-232 serial communication for PC to DSP board communication.
- 5V DC power supply.

6.4 Compiler Software

The programming of the target system was done in ANSI-C language. As a high level language it uses a compiler to translate the source code to machine-readable code, the binary code. See Appendix B for the procedure on how to programme the DSP Flash RAM.

The compiler development environment is made up of the following file system to perform the Compile -Link-Program Routine (CLP).

Compile.bat file

Compile.bat is the command to start compiling the program code. The compiler links the run.c code with the included header files (with file suffix .h). Compiling generates the following files with the following file suffixes and links the entire executable files to produce a run.out file:

- *.asm is the assembler code generated
- * .lst is assembler code with print layout and line numbers
- * .err is the error information if compiling was not successful.
- Run.obj file is the compiler user code that is generated as a result of a successful compilation.
- * .map is the memory allocation configuration and all global variables
- *.cmd is the file that contains all the *.obj files that are not generated by the compiler but are needed to run the project.
- *.inf is the information about section size and memory allocation
- Run.out is the executable file generated by linking the executable files with Run.obj.

Con_Prg.bat file

Con_Prg.bat is the command that starts the hex converter and the serial programmer using the Run.out file to program DSP flash RAM.

6.4.1 Compile-Link- Program (CLP) Routine common errors

- Folder path problem, CLP runs the run.c code in the same folder with Compile.bat file. So to run a new code one has to replace the old run.c code in the correct folder with the new one. If the new code is saved in a different folder the CLP will run the old one.
- When using interrupts one has to replace branch.obj with ints.obj in the .cmd file. Branch.obj is invoked by the linker to perform a simple jump to start address of the running program, whereas an interrupt is a jump to a specific address in the program memory.

6.5 Interface Boards

Interface boards were made for interfacing high power signals with the DSP board. The

243_DSP board can only operate with signal within 0 to 5V. This section describes the interface boards used for building laboratory UPS prototype.

6.5.1 DSP Interface Board

The DSP interface board allows a direct connection of signals to and from the DSP board. Figure 6-2 shows the interface board rooted on the DSP board on a stand. Power supply to the DSP board and other interface boards is supplied through this board. Four signal samples where required to implement closed loop control of the line-interactive UPS design.

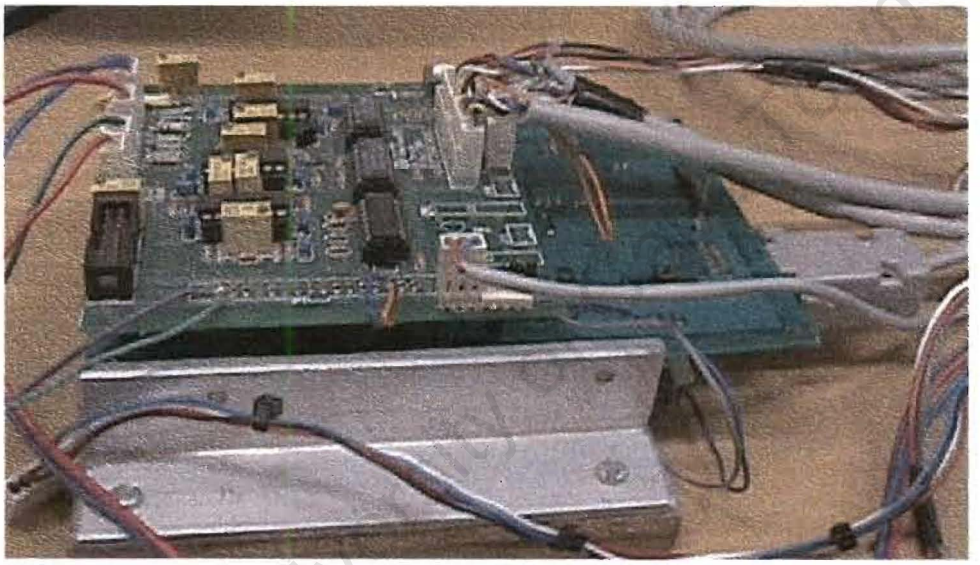

Figure 6-2: DSP interface board

The author was provided with a single-phase DSP interface board with no components on it. The author had to modify the board for a three-phase inverter switching and soldered all the components on to the board. The board is made up of several circuitries for DSP board protection.

Some of the important circuits on the board are:

- Operation Amplifier (OpAmp) circuits for reading four analog signals samples to the ADCs on the DSP board. The OpAmp circuits are made with an adjustable gain.
- 2.5V dc offset circuit for allowing negative signal to be read to the ADCs. This means that the reference voltage for the ADCs is 2.5V. Therefore a maximum positive peak of 2.5V and a minimum negative peak of -2.5V can be read to the ADC, since the DSP range is 0V to 5V.

6.5.2 Inverter Driver Board Interface Board

A three-phase IGBT inverter, driven by a semikron SKH160 driver board was used for building the UPS prototype. The semikron driver board requires 15V signals to drive the inverter, but the DSP operate in the range of 0V to 5V. Therefore an interface board shown in figure 5-3 was required. The wiring diagram of this interface board is shown in Appendix C.

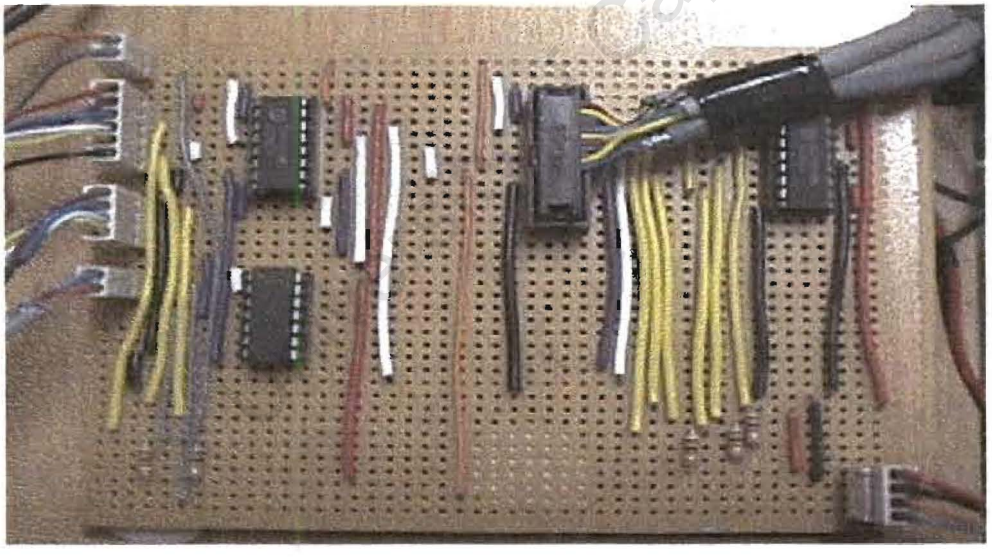

Figure 6-3: Inverter Driver Board Interface Board

On the board are two level shifters (CD4504BE) which convert signals from the DSP board from 5V to 15V range. Also IGBT switches protection signals from the driver board

to the DSP are connected through a level shifter to get 15V to 5V range. The level shifter acts as buffer providing protection and isolation to the DSP board.

The protection signals stop the switching of top and bottom IGBT switches at the same time. The driver board also has hardware protection that allows a 6 μ seconds delay on the switching of top and bottom IGBT switches.

Also on the board is MM74HC14N hex inverter chip providing two PWM signals directly from the DSP board. Since four PWM signals were provided from DSP interface board as it was made to operate a single-phase inverter, but six space vector PWM signals were required from the DSP board for three phase inverter switching.

6.5.3 Signal conditioning Board

The DSP operate on 0 to 5V range. The four sampled signals namely, DC bus 160V, supply voltage 150V, load voltage 220V and battery charging current were way out of the DSP range. As means of safety to the author it was found necessary to keep the high power signals away from the interface board. Since the author's hands were constantly in contact with the DSP interface board, taking readings and debugging the C programming code. This lead to the construction of signal conditioning boards shown in figure 6-4.

LEM, current and voltage transducers (LA 25-NP and LV 25-P) were used for signal conditioning. LEM modules were chosen for their excellent linearity and they provide isolation to the two signal ranges.

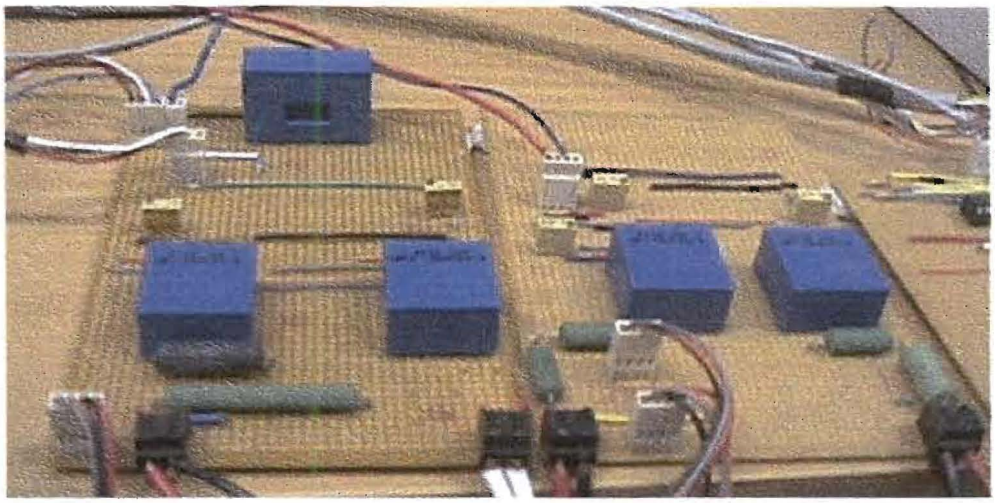

Figure 6-4: Signal conditioning Board

6.5.4 Static switch

A static thyristor switch was used for isolating the mains supply voltage from the UPS when supply voltage magnitude went below the required minimum value. This would stop the UPS from feeding into mains supply. The DSP measured the magnitude of the supply voltage and sent a signal to switch off once voltage went below the minimum value.

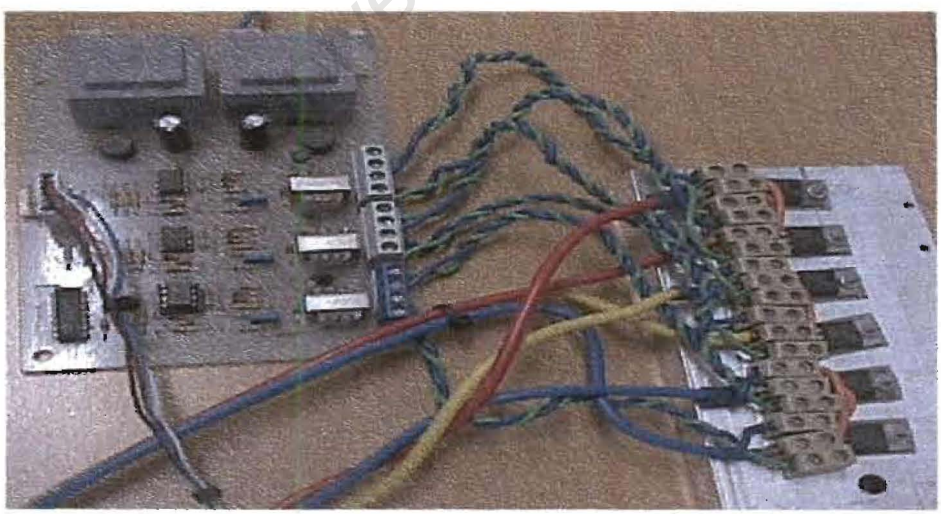

Figure 6-5: Static Switch

Figure 6-5 shows the static switch that was made by a company called MLT drives. The wiring diagram of the switch is shown in Appendix B. A month was almost spent trying to get the thyristor switch to function properly. The main problem was the drawings were different from the built switch, so tracing the mistakes on the board was not easy. When the switch got to function, it would only turn off when the supply current was less than 5 amps. Above 5 amps, the pulse to isolate the UPS would fail. Turn off snubber circuits designed failed to switch off the static switch as required. Thyristors were getting too hot and failed to switch off.

The heat sink on which the static switch thyristors are mounted must be changed. A heat sink that keeps the thyristors within their operational temperature should be found or find thyristors that can operation in that temperature conditions.

7 Software Description

7.1 Introduction

This chapter describes the program that implement a closed loop control of a line-interactive three to single phase UPS system using the TMS320F243 DSP. The programming was carried out in C-programming language and it uses four ADCs to instantaneously sense four signals from the UPS system. The figure below shows the control block diagram of the UPS. The program was developed with the help of example programs that came with the DSP board.

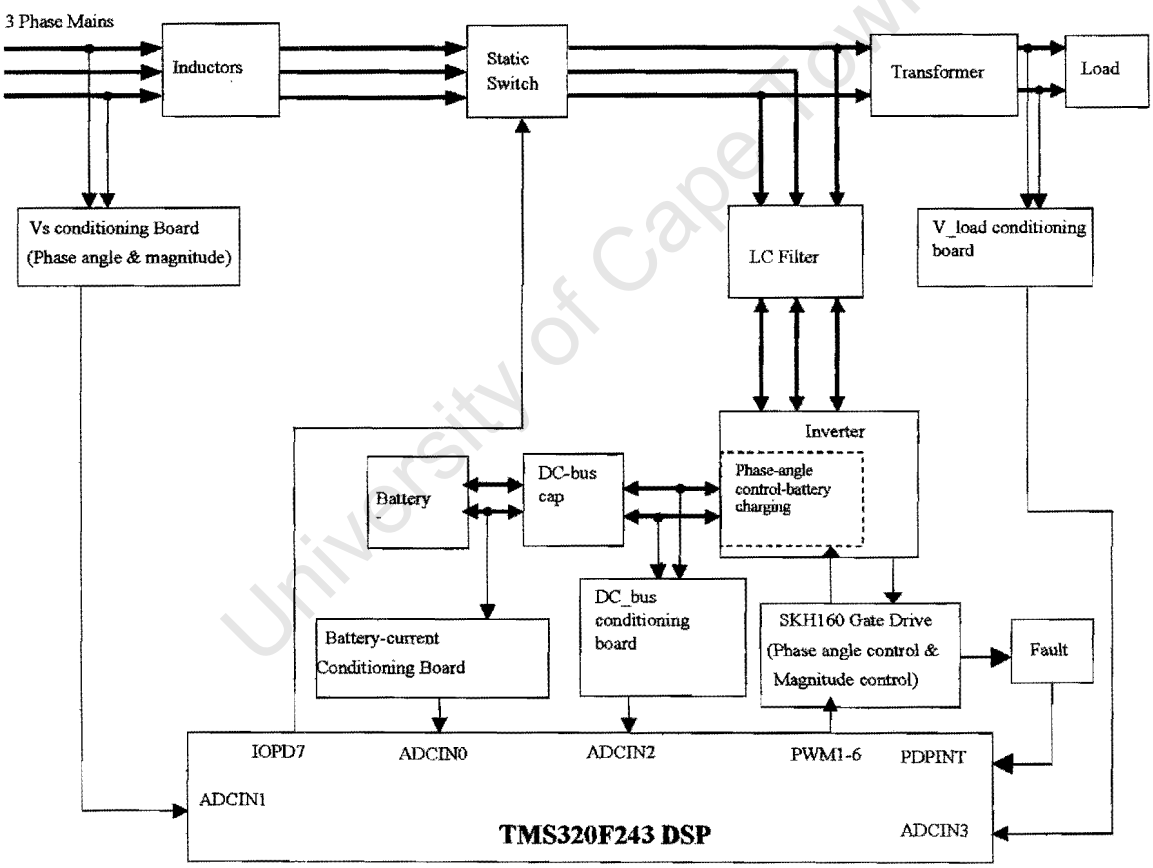

Figure 7-1: UPS Control Block Diagram

7.2 Program Structure

The program structure is based on the control sampling cycle of general-purpose (GP) timer 1. Timer 1 provides the time base for PWM generation, ADC sampling and all the control loops. The switching frequency of timer 1 is 10kHz, which gives a period of 100micro-seconds. The timer operates in continuous up/down counting mode. Interrupt mask registers IMR and EVIMRA are configured to allow timer 1 to generate an interrupt on underflow (when timer 1 value is zero).

Timer 2 is the time base for the internal generated sine wave. The period of the counter is scaled to give a switching frequency of 50Hz. The timer operates in continuous up counting mode.

7.2.1 Main Program Flow Chart

The flow chart of the main program in shown in figure 7-2. Software initialisation of all variables is done first. Then desirable registers and interrupts are enabled. Unused interrupts are masked, then timer 1 and timer 2 are started. The program loops in the background routine performing all non-time critical functions. The background routine is the main program loop that ensures that the program has defined bounds. The program code is shown in appendix C.

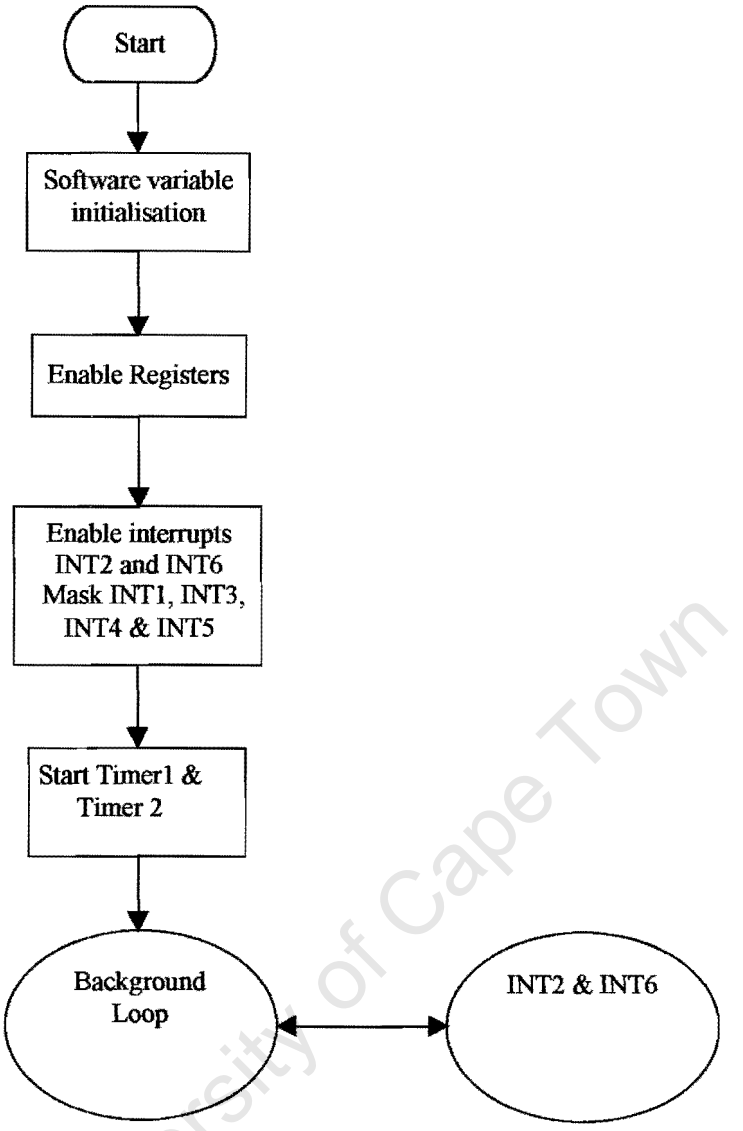

Figure 7-2: Main Program Flow chart

7.2.2 Interrupts

Two interrupts INT2 and INT6 occurring on different interrupt levels have been defined. The interrupts are executed and completed within the switching cycle time frame. When CPU is interrupted the background operation is stooped and the interrupt level is determined. A context save of important registers is carried out, and then it branches to the corresponding interrupt service routine. The process is illustrated in the flow chart in figure 7-3.

INT2 Interrupt Dispatcher Flowchart

INT2 interrupt source is Timer 1 underflow interrupt only. When INT2 is determined the program branches to timer 1 underflow interrupt service routine (ISR). The flowchart is illustrated in the figure below.

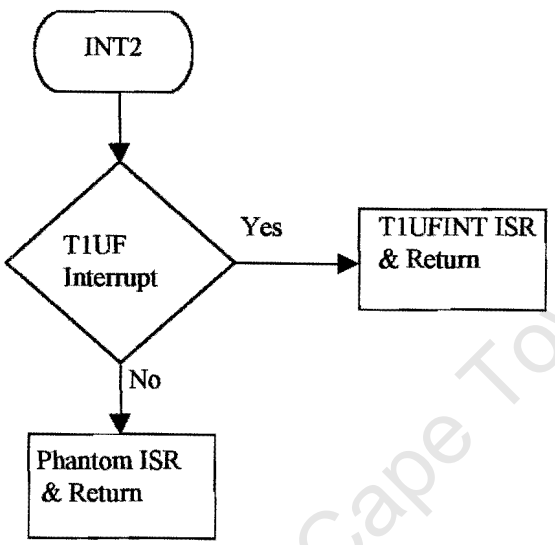

Figure 7-3: INT2 Interrupt Dispatcher Flowchart

Interrupt Service Routine

In the routine, the program reads all the ADCs and all control loops are carried out. When there is normal mains power supply, the program executes a phase locking algorithm to phase lock to the supply voltage and it executes a phase angle technique algorithm to regulate the dc bus and battery charging. The code also regulates the load voltage. On power failure the program phase locks to the internally generated phase angle and does not execute the phase angle technique algorithm. It also switches off the static switch. Figure 7.4 illustrates a simplified flowchart.

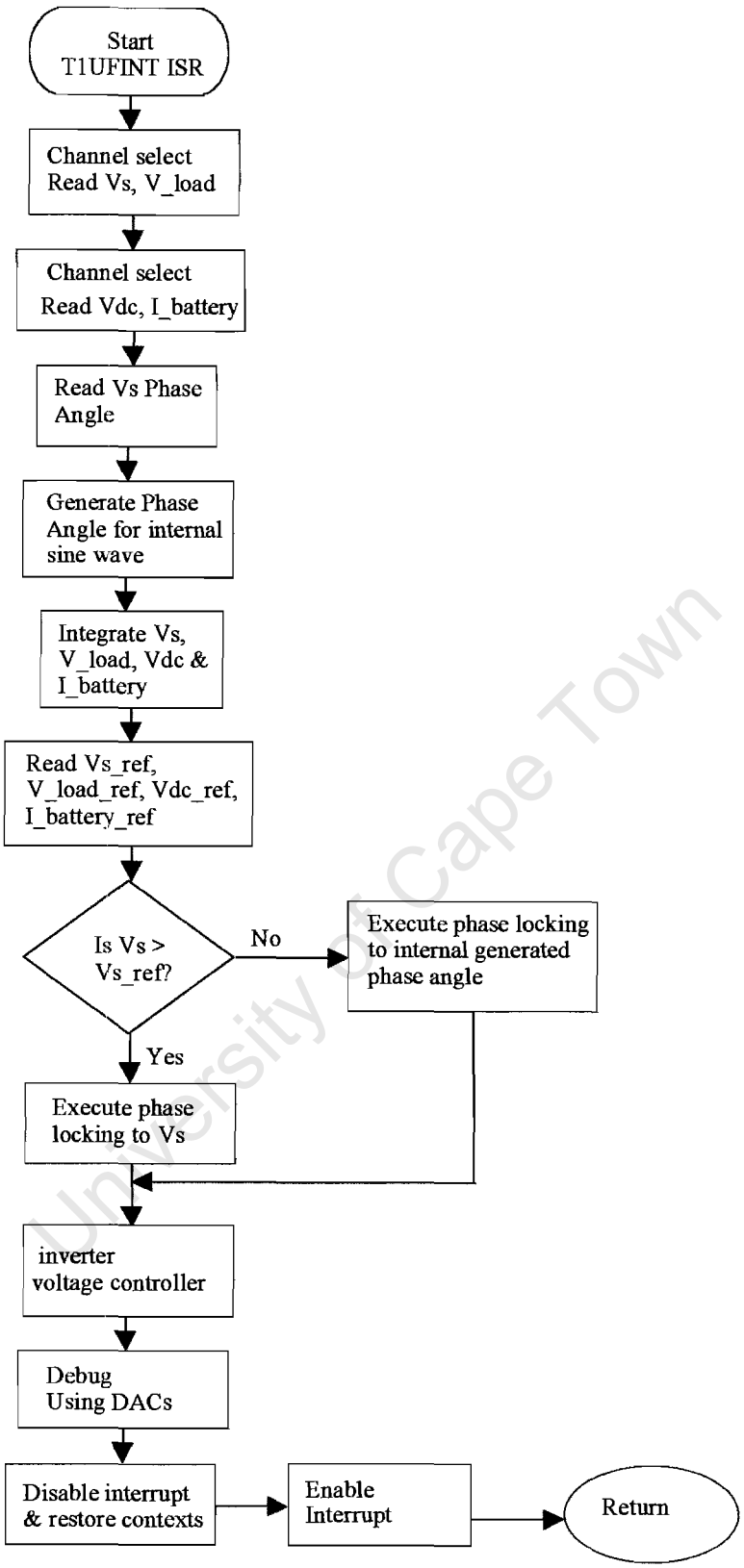

Figure 7-4: Interrupt service routine flowchart

Detailed inverter voltage controller from the above flowchart is illustrated in figure 7-5 to show how space vector PWM was generated. A detailed description on how to generate space vector PWM is described in chapter 5.

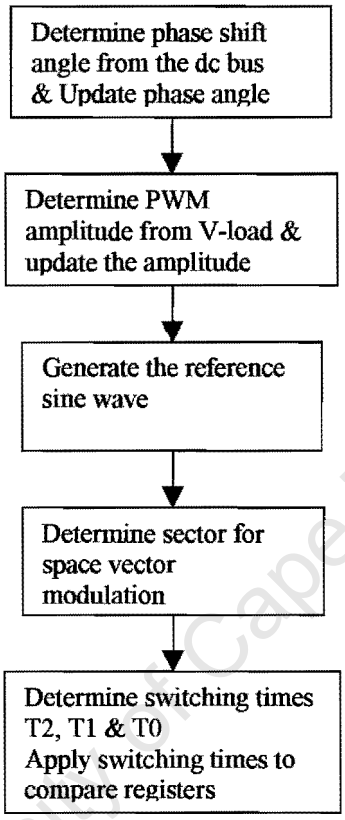

Figure 7-5: Inverter voltage controller

7.3 Phase Locking

LEM voltage transducer (LV25-P) was used for voltage conditioning. Supply voltage is conditioned from 150V to 5V and is read to the DSP board though ADCIN1. To determine the phasor angle the sampled Vs waveform is split into Vs_real and Vs_imaginary, by sampling the same waveform 90 degrees later. The waveforms of Vs_real and Vs_imaginary read from the DACs are shown in the figure below.

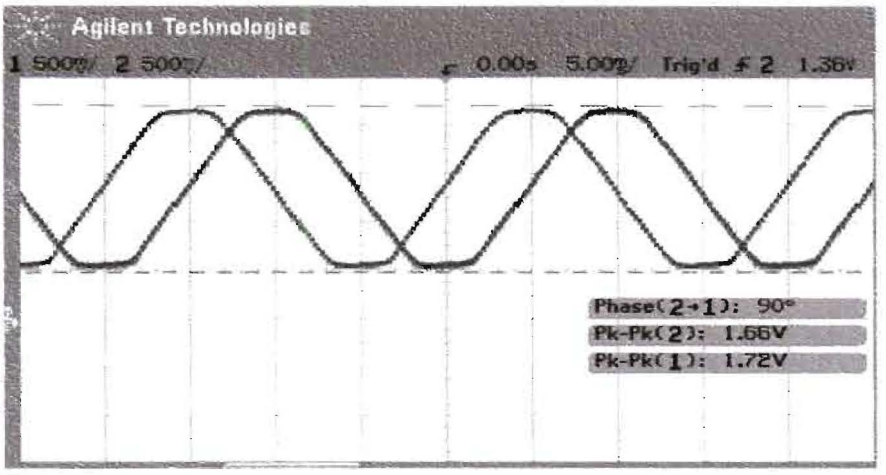

Figure 7-6: Vs_real and Vs_imaginary

The angle is then determined by an arctan operation on Vs_real and Vs_imaginary. The calculated angle is the then used as the base angle to generate the reference sine wave for space vector generation. Therefore the space vector generated inverter output is phase locked to Vs, since the reference sine wave is always in phase with Vs.

To obtain fundamental frequency inverter output is filtered. The LC filter introduces a phase shift to the inverter output. To compensate for the phase shift an angle of same value but opposite sign is added to the base angle.

Three reference angles are required for three-phase inverter switching. The other two phases are generated by adding 120 and 240 degrees to phase A. The figure 1-7 shows phase A and Phase B read from DACs.

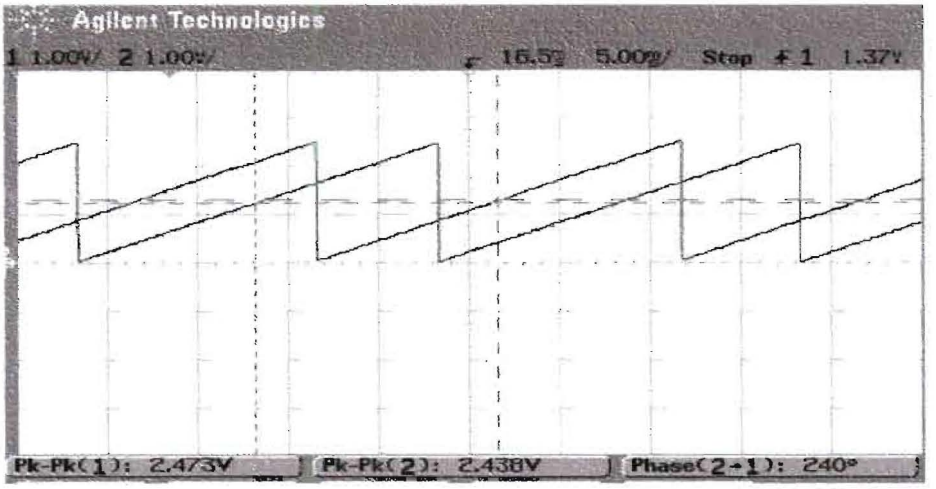

Figure 7-7: Phase A and phase B read from DACs

8 Laboratory UPS Experimental Results

8.1 Introduction

A 2.5 kVA three phase to single phase laboratory UPS prototype was built and tested. The inverter used to build the UPS is capable of delivering 120kVA. More power could be delivered from the UPS if a higher dc bus is used and charging some of the equipment to the right power rating. The experimental results are presented here to validate the proposed UPS topology. The laboratory UPS prototype picture is shown in figure 8-1 and UPS power circuit diagram is shown in figure 8-2.

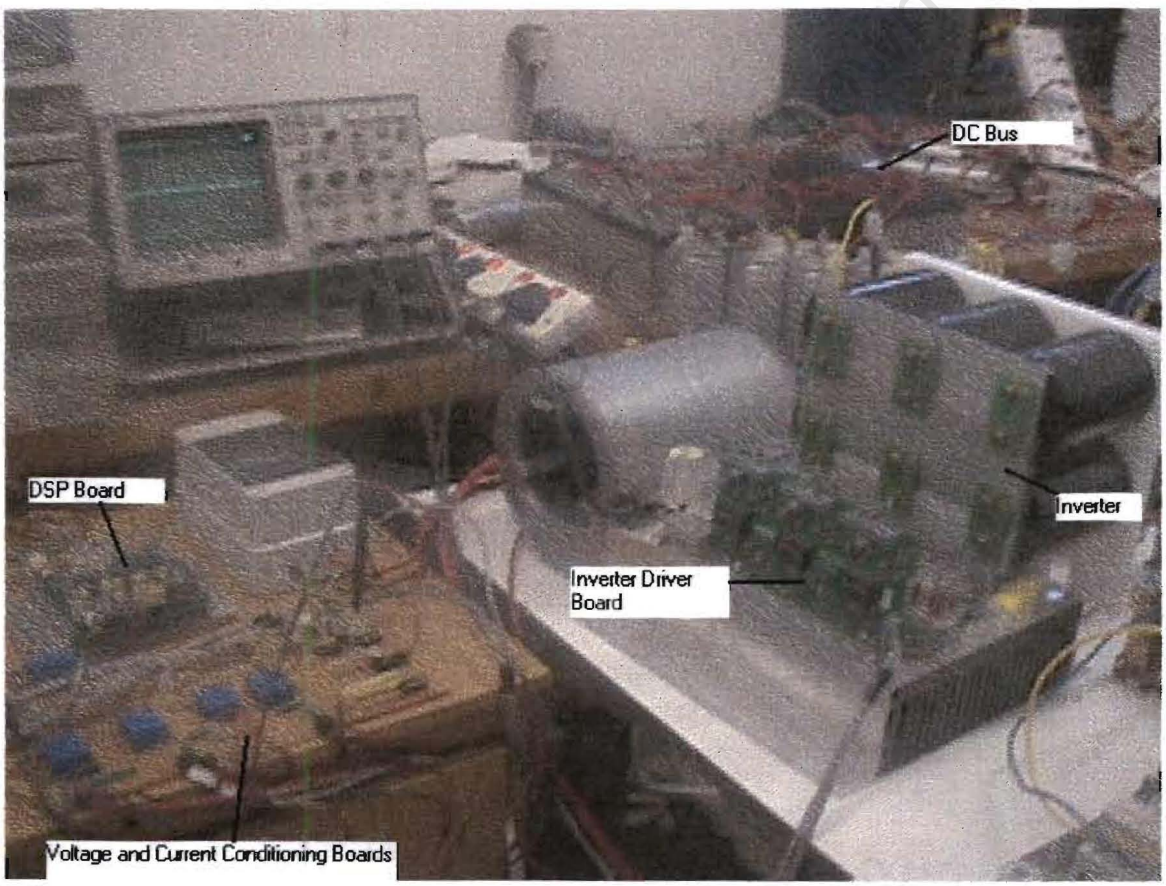

Figure 8-1: Laboratory UPS prototype Picture

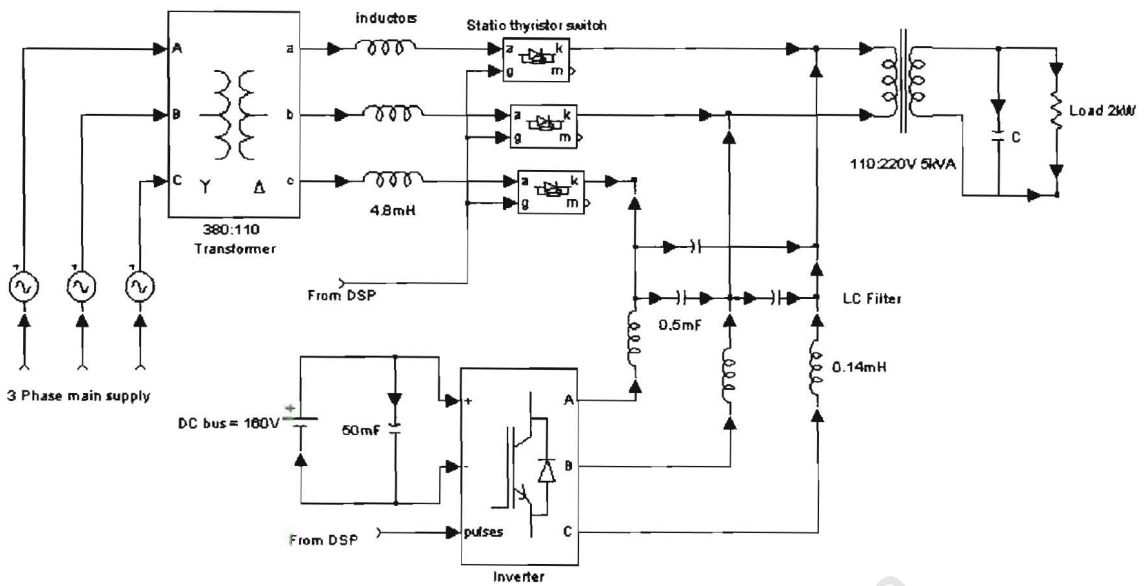

Figure 8-2: UPS power circuit diagram

The following equipment was used to build the UPS:

- Variable transformer for setting supply mains voltage to a specific value and also to isolation UPS from the mains
- Three 4.8mH link inductors
- Static thyristor switch
- Three 50 μ F capacitors for filtering inverter output
- Three 0.14mH inductors for filtering inverter output
- Semikron IGBT inverter driven by SKH160 IGBT driver board (SKM200GB 123D). The current and voltage rating of inverter is 200 amps and 600V.
- DC bus made up of 14 lead acid 12V 7AH-batteries.
- DC bus smoothing cap.
- 110 to 220 step up transformer
- 2kW resistive load
- Digital power meter Yokogawa (WT1600) and a two-channel 100MHz Agilent mixed signal oscilloscope (54622D) were used for measuring signals.

Digital power meter Yokogawa was used for measuring three phase signals. Three-voltage, three-current (3V3A) wiring method was used [16]. U1 to U3 and I1 to I3 are the

supply voltages (Vs) and currents (Is). U4 to U6 and I4 to I6 are the filtered inverter output voltages (Vups) and currents (Iups).

8.2 Space Vector PWM Results

The software and hardware was tested to check if it was operating as intended before switching the inverter. DACs were used for debugging the code. The fundamental space vector (SV) PWM was checked by filtering the PWMs after level shifting. Figure 8-2 shows two of the three line to neutral SV PWM outputs. The carrier frequency was taken out by RC low pass filter. Figure 8-3 is the difference between two waveforms, representing the line to line voltage waveform. The waveforms generated by the DSP correspond to the theoretical excepted waveforms.

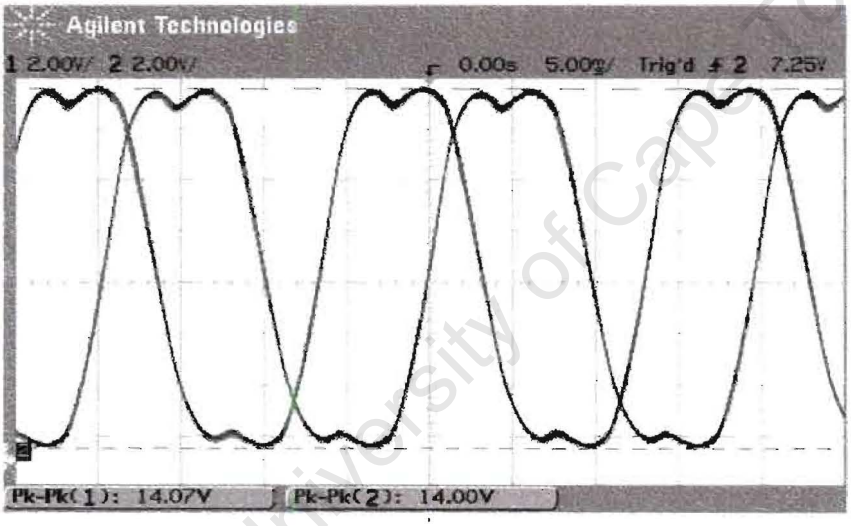

Figure 8-3: Line to neutral SV PWM outputs with carrier filtered out

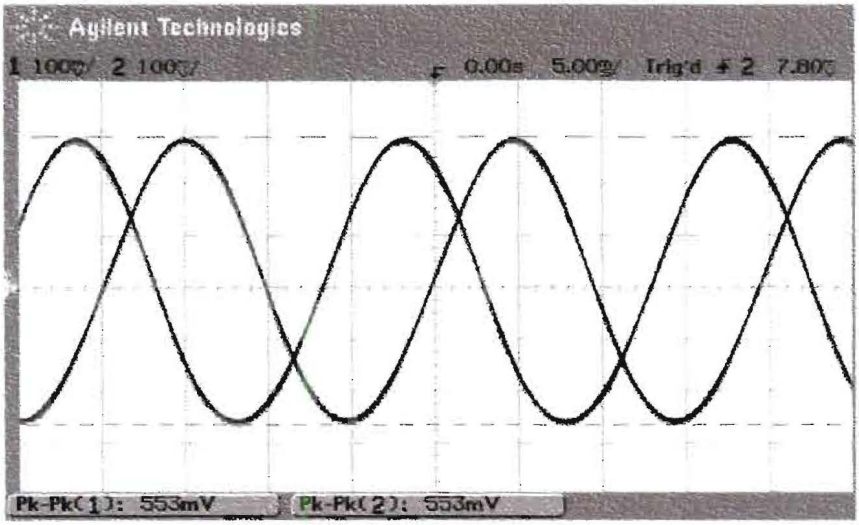

Figure 8-4 Line to line SV PWM outputs with carrier filtered out

8.3 Phase Locking Results

Phase locking was achieved by calculating the phase angle of the sensed line to line voltage, then using the angle to generate space vector PWMs. The other two phases were generated by adding 120 and 240 degrees to the calculated phase angle. Figure 8-4 shows the line to line supply voltage and the phase angle read from a DAC.

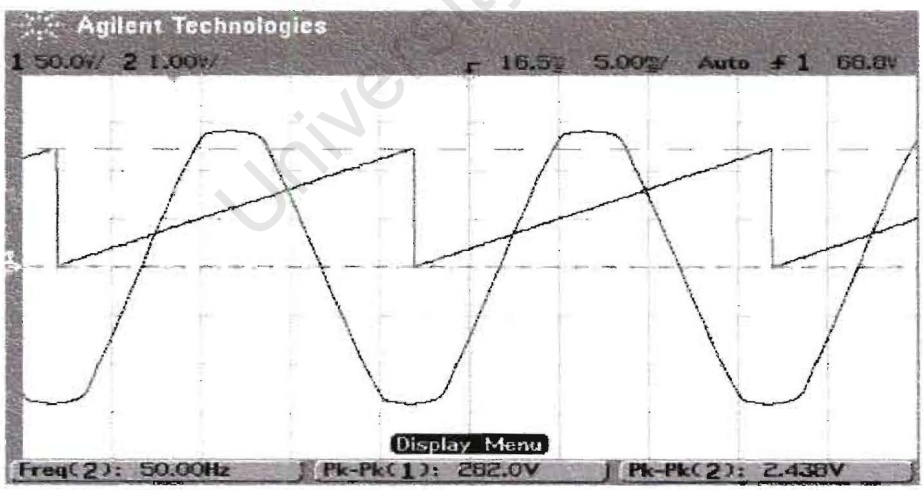

Figure 8-5: Supply voltage and the phase angle read from DAC

Supply three-phase voltage was connected to the three-phase inverter output once the corresponding lines were of same magnitude and phase locked. The figure below shows the filtered inverter output voltage phase locked the supply voltage. The supply voltage magnitude is bigger than the inverter voltage.

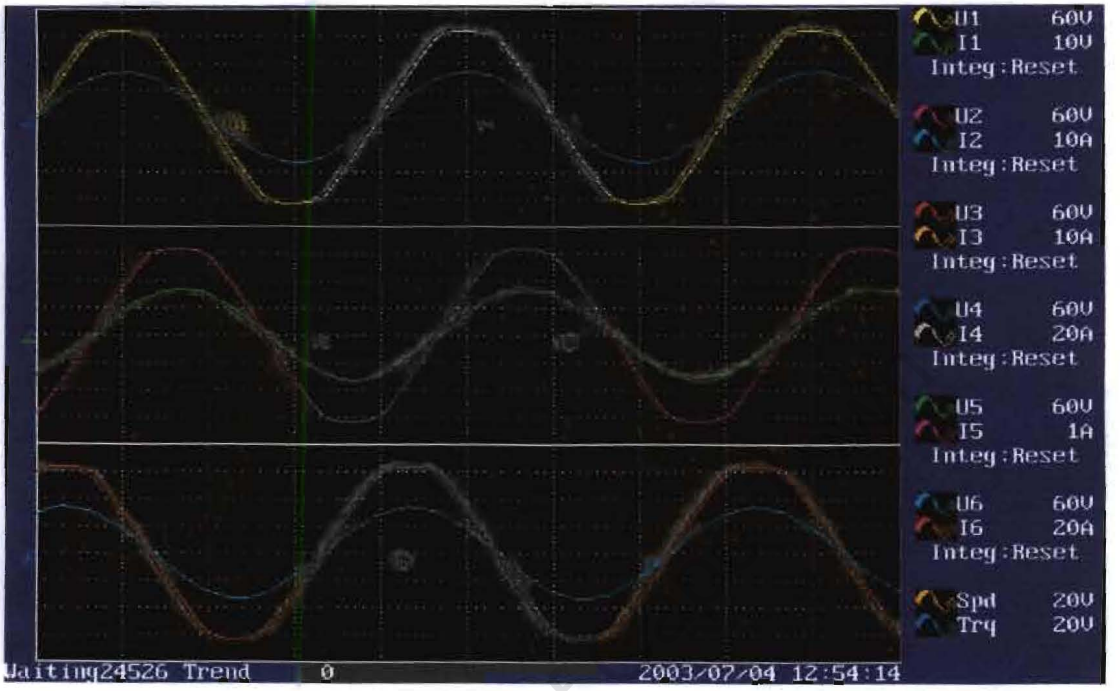

Figure 8-6: Inverter output phase locked to the Supply voltage

Once the voltages were phase locked and were of same magnitude, the inverter voltage was then phase shifted so as to draw current from the supply. The figure below shows the inverter output voltage phase shifted by 30 degrees.

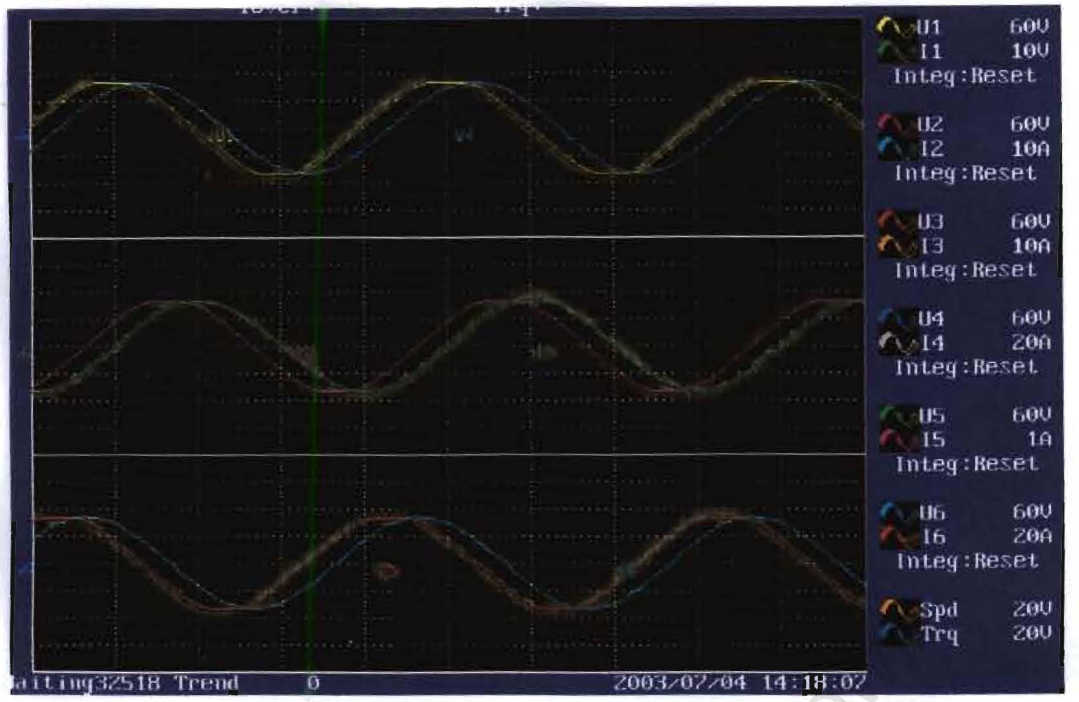

Figure 8-7: Inverter output voltage phase shifted by 30 degrees

8.4 Voltage regulation results

During normal power supply and when the batteries are fully charged the dc bus (Vdc) was regulated at constant voltage, by increasing or decreasing Vups phase angle with respect to Vs phase angle. The angle is increased to draw more current from the mains supply when the load is increased and vice versa. The figure below shows the results when Vdc was regulated at 170V, Vs = 100V and Vups at 107V. Vups is phase shifted from Vs by about 10 degrees.

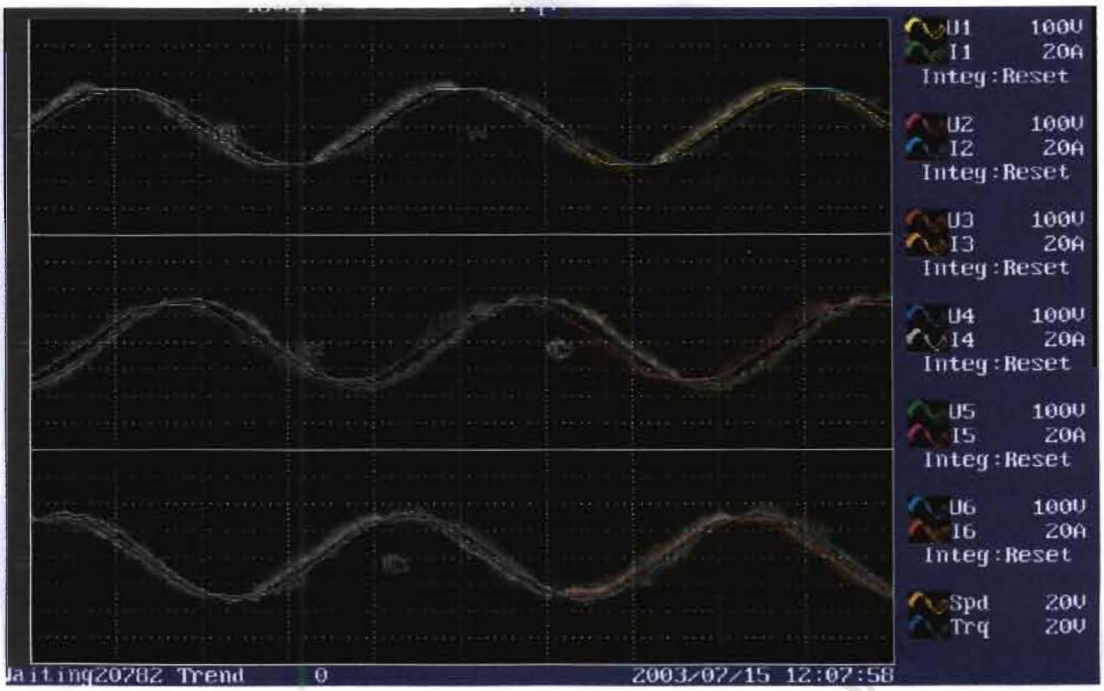

Figure 8-8: Vs and Vups during voltage regulation.

The figure below shows supply currents during voltage regulation. The supply three phase currents are almost equal. The average value of the three-phase supply current is 14.8A. The supply currents are equally displaced, about 120 degrees apart.

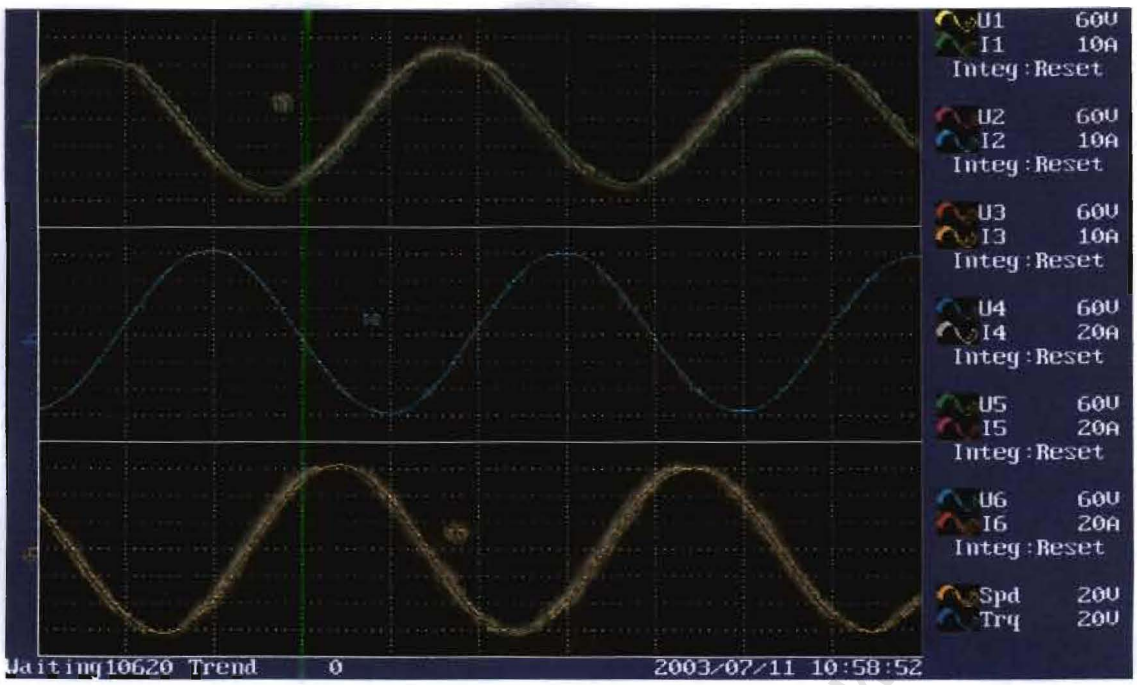

Figure 8-9: Is during voltage regulation

The figure below shows UPS currents (Iups) during voltage regulation. The UPS is supplying a parallel combination of single-phase loads. The load is connected across U4 and U6.

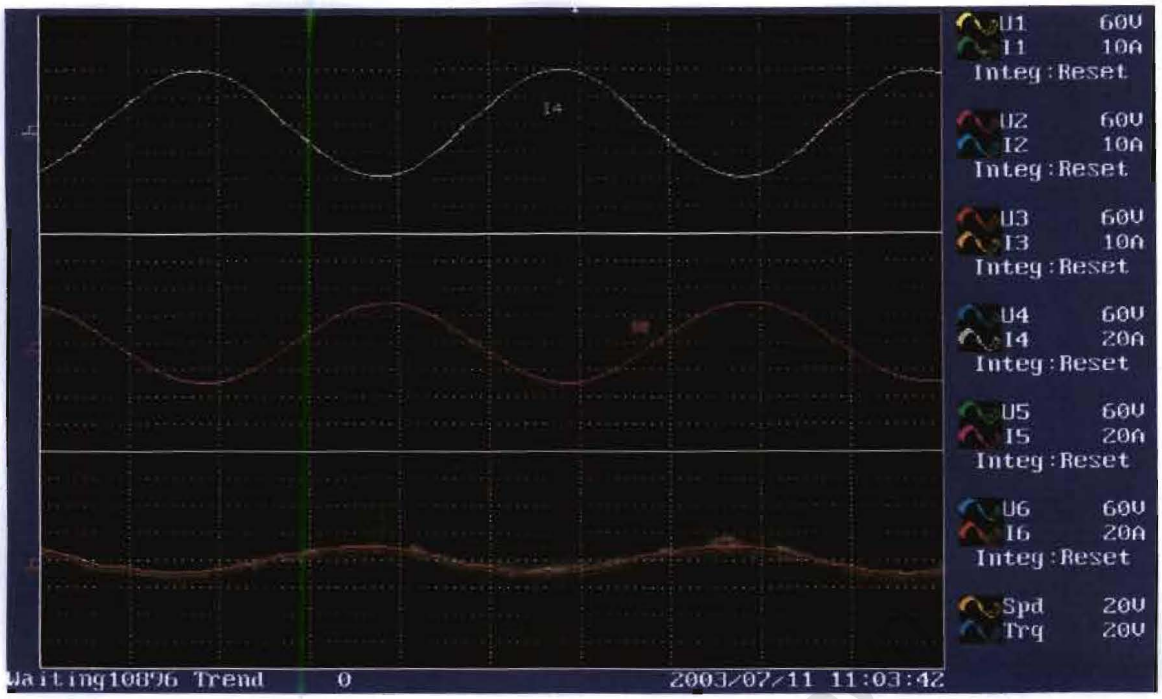

Figure 8-10: Iups during voltage regulation

The figure below shows the voltage across a 2kW load and the respective current. The current is in phase with the voltage since the load is resistive.

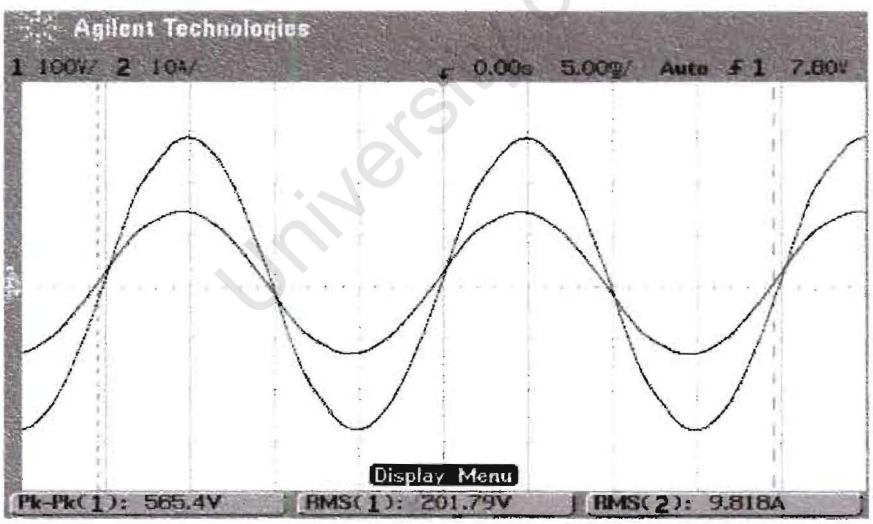

Figure 8-11: V_load and I_load during voltage regulation

The numerical results of voltage regulation are shown below. From the results it can be seen that the supply three phase voltages are not exactly the same and the waveform is flat topped. It can be argued that the phase angle between the three phases is not exactly 120 degrees as assumed. Although phase locking is achieved by calculating the phase angle of one phase, and assuming that the phases are 120 degrees apart. The effects of the phases not exactly 120 degrees apart and the slight difference in supply voltage magnitudes affected Is and Vups. This caused the small difference in Vups line to line voltage magnitudes, resulting in a slight imbalance of Is currents.

An effective way of providing load balancing, the three phase supply currents can be sampled, then use phase angle technique to keep their magnitudes equal and equally displaced, 120 degrees apart.

The overall three-phase supply power factor is 0.9828. Unit power factor is achieved when the Is currents are almost equal to Iups as explained in chapter five. Better power PF can be easily achieved by balancing the current in Phase A and phase C.

From the figure below (ΣB) it can be seen that the inverter is absorbing zero real power during voltage regulation as expected from the theory.

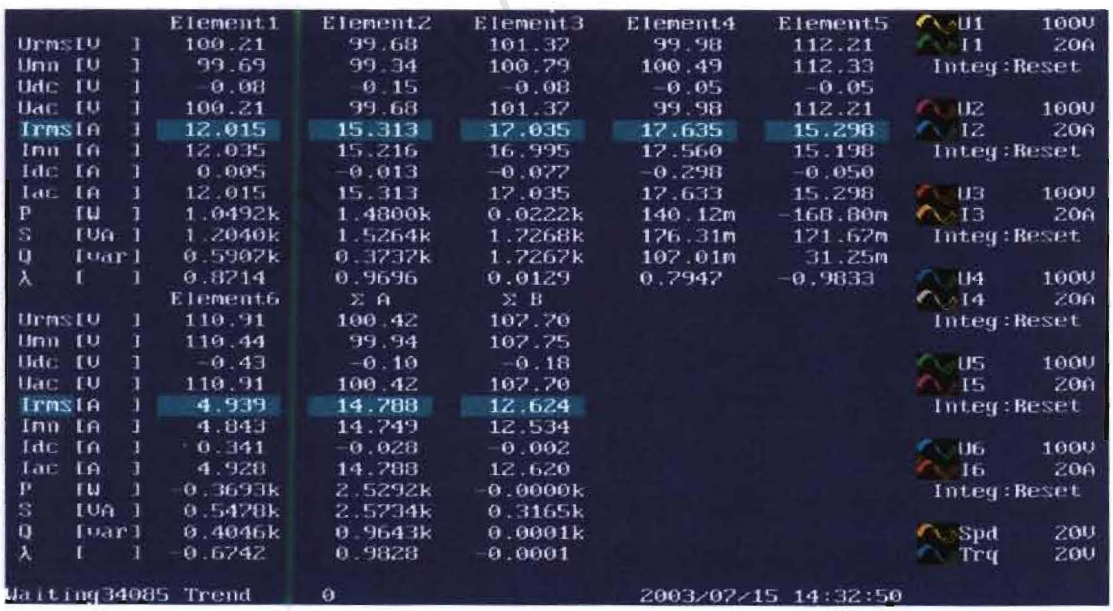

Figure 8-12: Numerical results of Voltage regulation

8.5 Battery charging results

Phase angle control is used to control the amount of power absorb by the UPS for battery charging. The figure below shows Vs and Vups during battery charging. The phase shift angle is about 18 degrees. Vdc is at 130V.

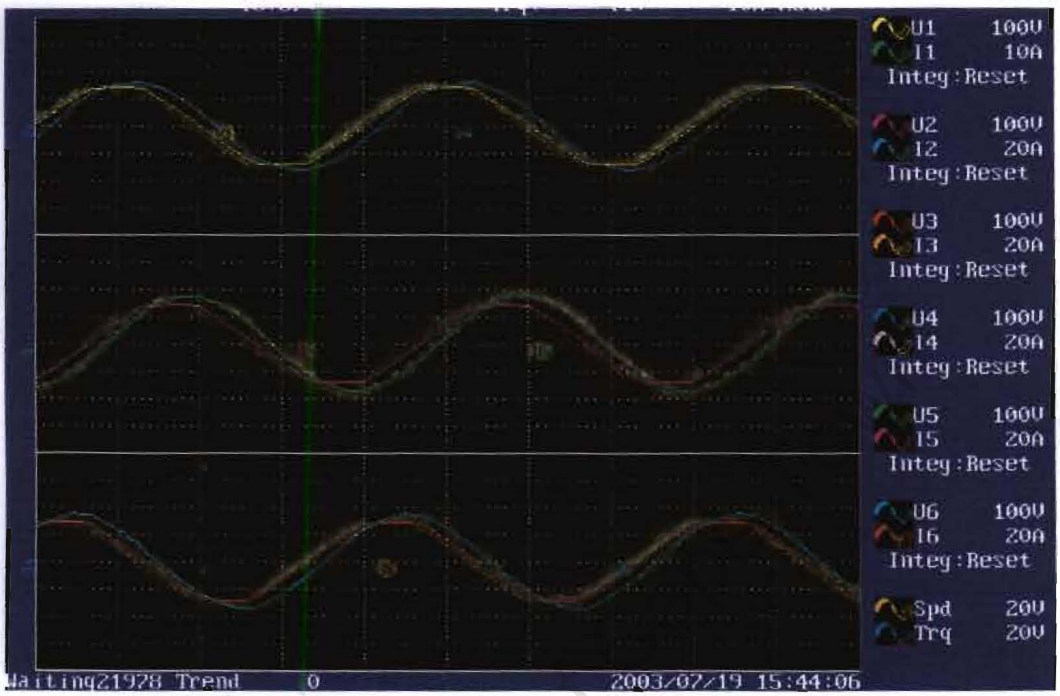

Figure 8-13: Vs and Vups during battery charging

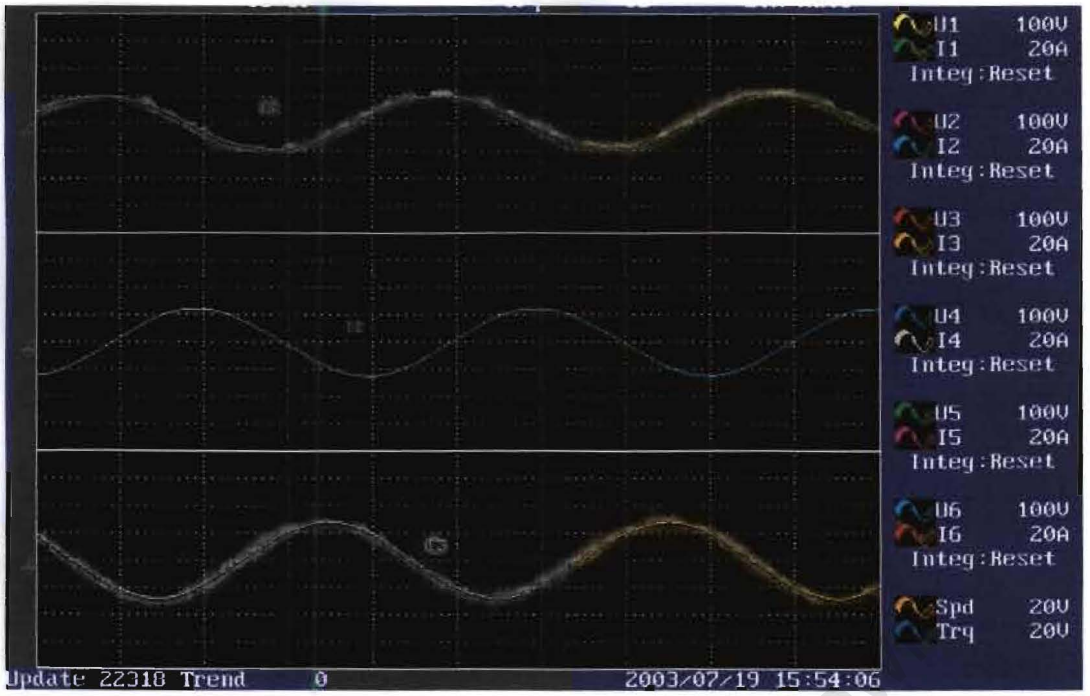

Figure 8-14: Is during battery charging

The numerical results of battery charging are shown below. The inverter is absorbing 413W from the supply and the rest is absorb by the load. The supply power factor is 0.9845.

	Element1	Element2	Element3	Element4	Element5	
Urms[V]	86.15	86.70	87.05	84.56	91.85	U1 100V
Umn [V]	85.87	86.56	86.65	85.38	91.51	I1 10A
Udc [V]	-0.02	0.02	-0.04	-0.03	-0.00	Integ:Reset
Uac [V]	86.15	86.70	87.05	84.56	91.85	U2 100V
Irms[A]	6.496	7.757	9.055	6.176	7.254	I2 20A
Imn [A]	6.583	7.744	8.929	5.996	7.243	Integ:Reset
Idc [A]	0.132	-0.014	-0.112	-0.541	0.020	
Iac [A]	6.494	7.757	9.054	6.152	7.254	U3 100V
P [W]	0.4972k	0.6513k	0.0036k	0.2985k	-0.7113k	I3 20A
S [VA]	0.5596k	0.6726k	0.7882k	0.5222k	0.7123k	Integ:Reset
Q [var]	0.2568k	0.1680k	0.2882k	0.4285k	0.0377k	
λ [ ]	0.8885	0.9683	0.0045	0.5716	-0.9986	U4 100V
	Element6	Σ A	Σ B			I4 20A
Urms[V]	90.23	86.64	88.88			Integ:Reset
Umn [V]	89.76	86.36	88.88			
Udc [V]	-0.05	-0.02	-0.03			U5 100V
Uac [V]	90.23	86.64	88.88			I5 20A
Irms[A]	1.971	7.769	5.300			Integ:Reset
Imn [A]	1.950	7.752	5.230			
Idc [A]	0.523	0.002	0.001			U6 100V
Iac [A]	1.900	7.768	5.269			I6 20A
P [W]	-0.1232k	1.1485k	-0.4128k			Integ:Reset
S [VA]	0.1778k	1.1665k	0.8154k			
Q [var]	0.1283k	0.4249k	0.4662k			Spd 20V
λ [ ]	-0.6925	0.9845	-0.5062			Trq 20V

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Figure 8-15: Numerical results of Battery charging

8.6 Power outage results

The converter only does a pure inverter function. It yields regulated load voltage without considering the phase angle of the inverter output voltage. The figure 8-15 shows the inverter output voltage, and figure 8-16 shows lups during power outage.

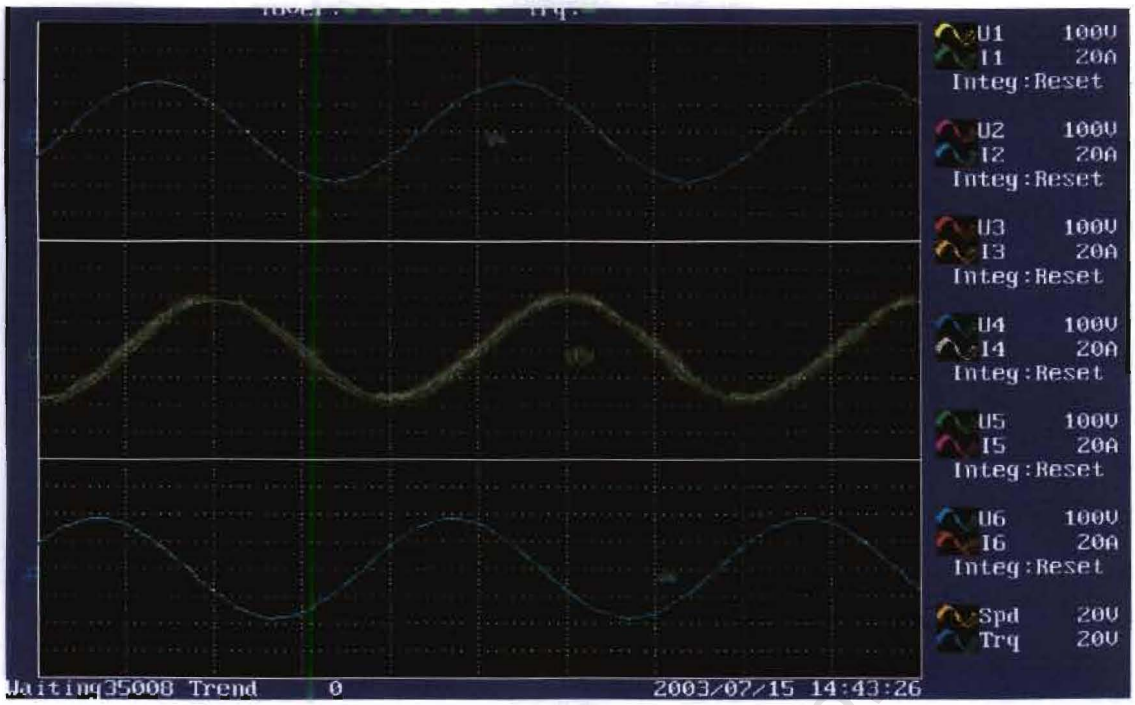

Figure 8-16: Inverter output voltage during power outage

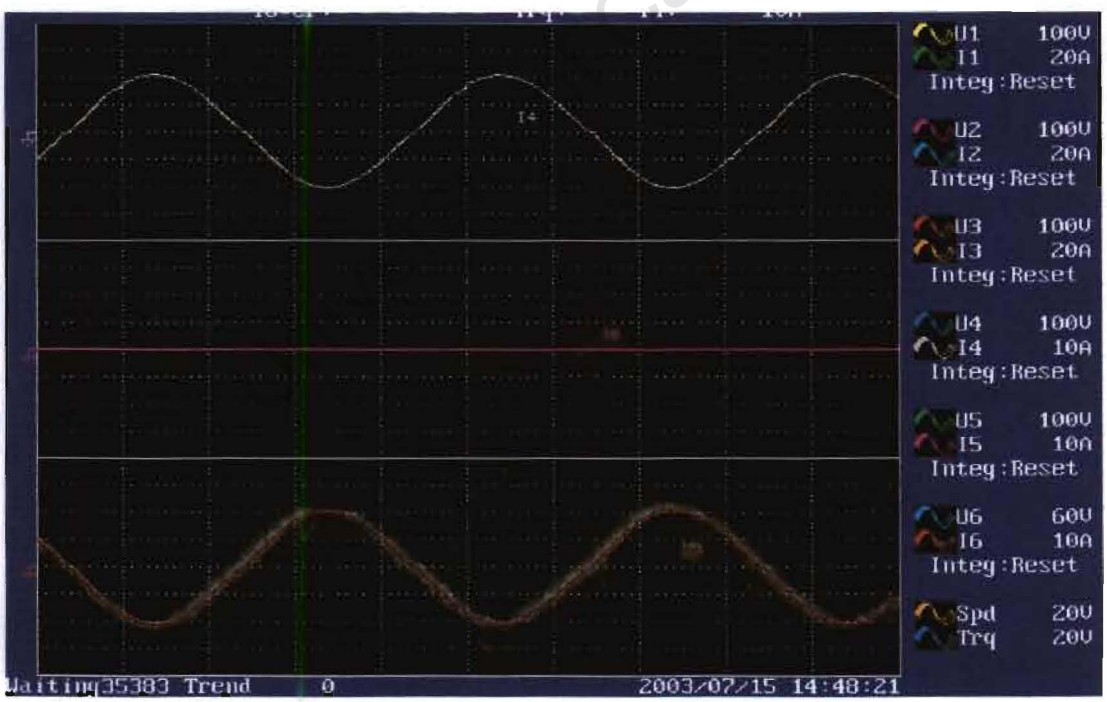

Figure 8-17: Iups during power outage

The figure below shows V_load and the corresponding current during power outage.

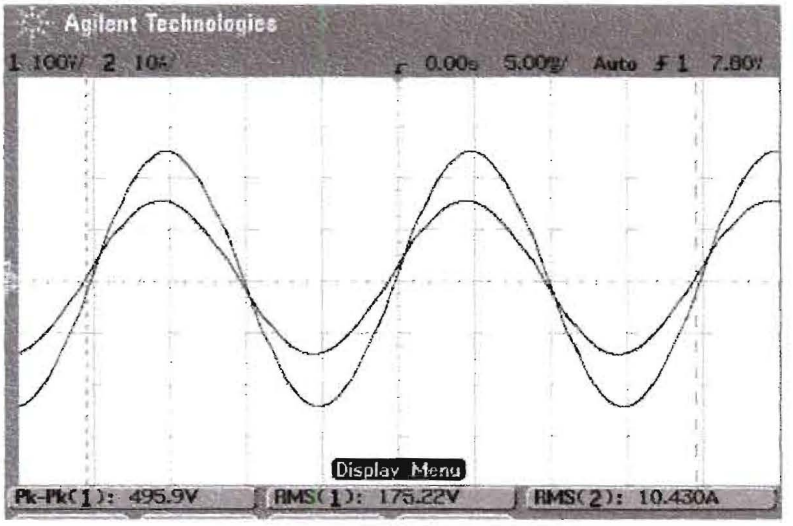

Figure 8-18: V_load and I_load during power outage

9 Conclusions

TMS320F243 DSP was used to implement a closed loop control of a three to single phase UPS. Based on the findings and results of the built laboratory UPS the following conclusions are made:

- SV PWM is easily digitally implemented. It offers a wide linear modulation range, which made the inverter output control easier.
- A robust phase locking of a three-phase system (phases 120 degrees apart) can be achieved by calculating the phase angle of one phase, then generate the other two phases at 120 degrees apart. Phase locking algorithm takes a lot of the DPS processing capacity. Calculating one phase of the three phases saves a lot of DSP memory, at the same time producing very good results.
- Phase angle technique can be used to bi-directionally control power through an inverter. Therefore allowing the inverter to be operated as a battery charger.
- Phase angle technique can be used to draw sinusoidal balanced currents from a three phase mains supply, and supply it to a parallel combination of single phase loads. An effective way of providing load balancing is to sample the three phase supply currents, then use phase angle technique to keep their magnitudes equal and equally displaced, 120 degrees apart.
- With careful selection of linking inductors size and phase shift angle, a stable UPS system with a very good power factor can be achieved.
- The UPS provides good mitigation of the power line problems. It improved the UCT flat-topped sine wave to a pure sine wave. It regulates the output voltage during normal operation (when power is supplied by the utility), and during power outage. Load voltage is regulated independently to the utility voltage without any interruptions.
- The proposed UPS design is particularly low cost due to its minimum need of magnetic and switching devices, compared to other high quality UPS.

10 Recommendations

Based on the findings and results of the DSP phase angle controlled three to single phase UPS project the following recommendations are made:

- It is recommended that the static switch heat sink be changed. A heat sink that would keep the thyrisotors within their operational temperature must be found, or find thyristors that could operation in those temperature conditions.
- Although the tests done on the UPS showed a successful operation of the UPS, more test are required at higher power rating.
- With the static switch operating, the dynamic response of the UPS to different electrical faults should be checked.
- The UPS was tested on pure resistive loads (light bulbs and heating elements), more tests must be done on different types of loads.
- For a better load balancing and to obtain unit power factor, supply currents should be sampled, then use phase angle technique to keep their magnitudes equal and equally displaced.
- To monitor the UPS, LCD display code should be added to the program code. The LCD can be used to display the following:

1. UPS mode of operation
2. Battery charging current and battery charging temperature.
3. DC bus voltage.
4. Mains supply voltage and UPS output voltage.
5. Supply power factor.

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APPENDIX A

Matlab Simulations

Single Phase Simulation Model

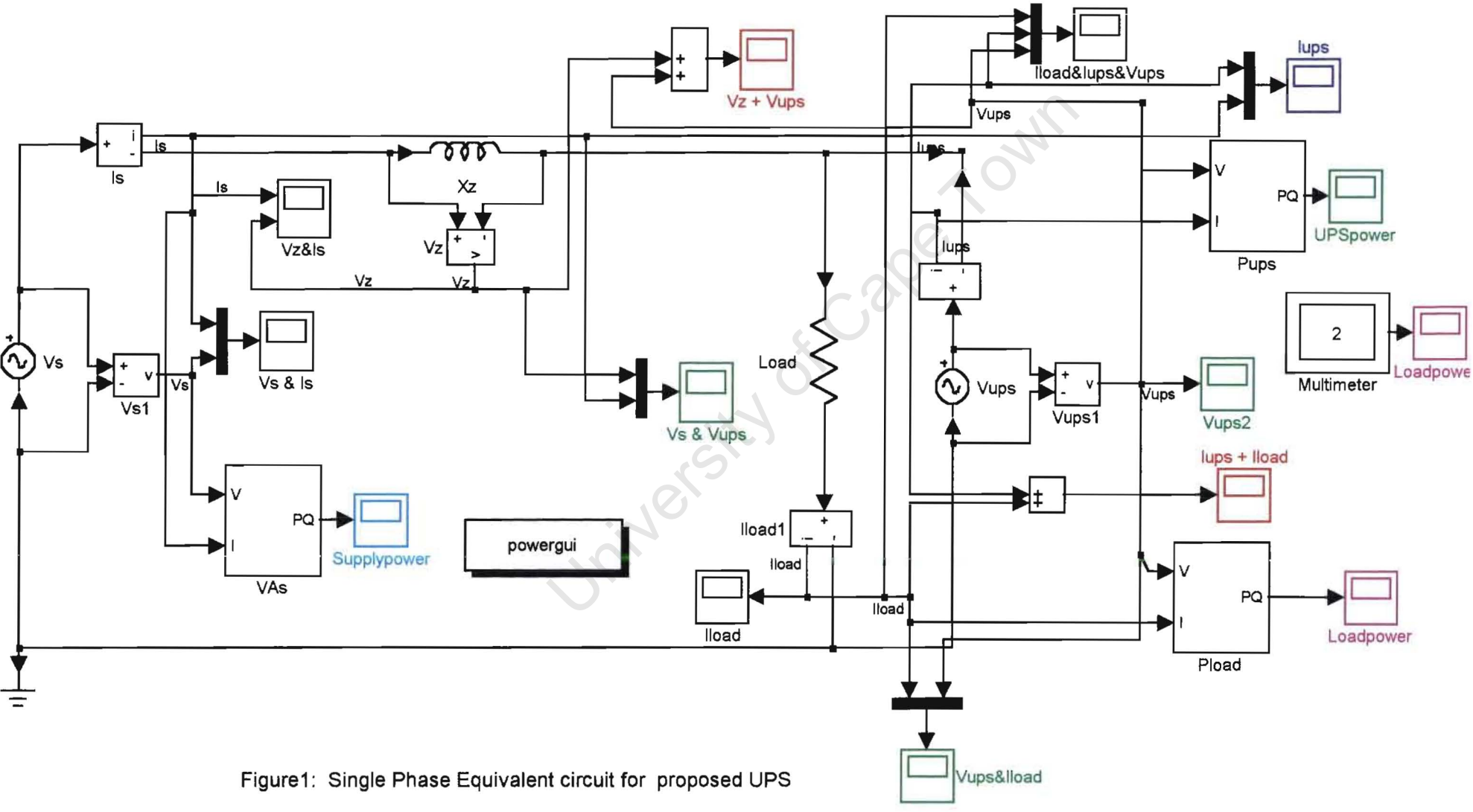


Figure1: Single Phase Equivalent circuit for proposed UPS

Single phase Matlab simulations

Simulations were carried out with a constant resistive load under the following conditions:

Load Power = 7.5 kW

Supply Voltage V_s = 220V

UPS Voltage V_{ups} = 230V

Load current I_{load} = 32.6A

Inductor X_z = 4.5 Ω

The voltage regulation point

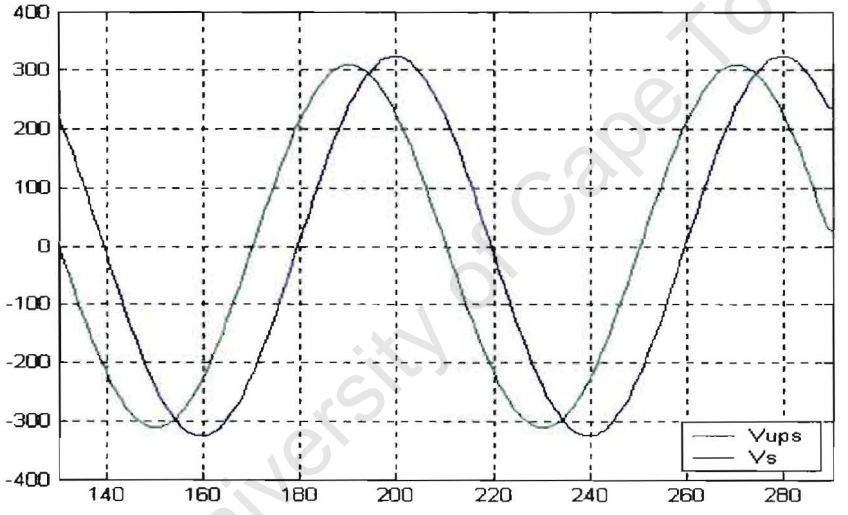


Figure 0-1: Vups lagging Vs by 42 degrees during voltage regulation

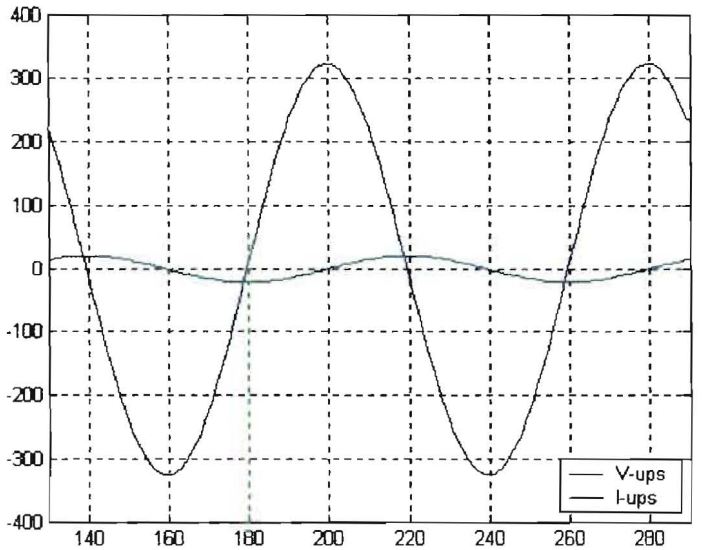


Figure 0-2: V_ups at 90 degrees to I_ups during voltage regulation, inverter absorbing zero real power

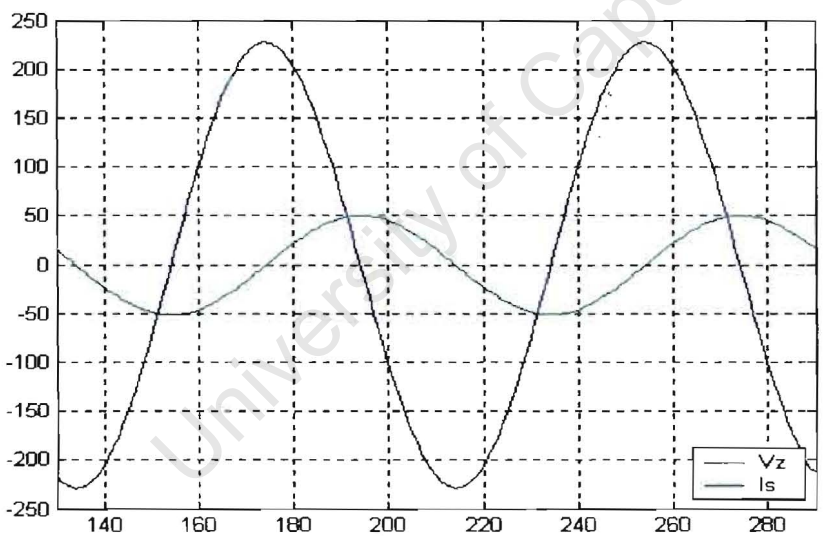


Figure 0-3: Sinusoidal current Is drawn from supply, Is lagging Vz by 90 Degrees

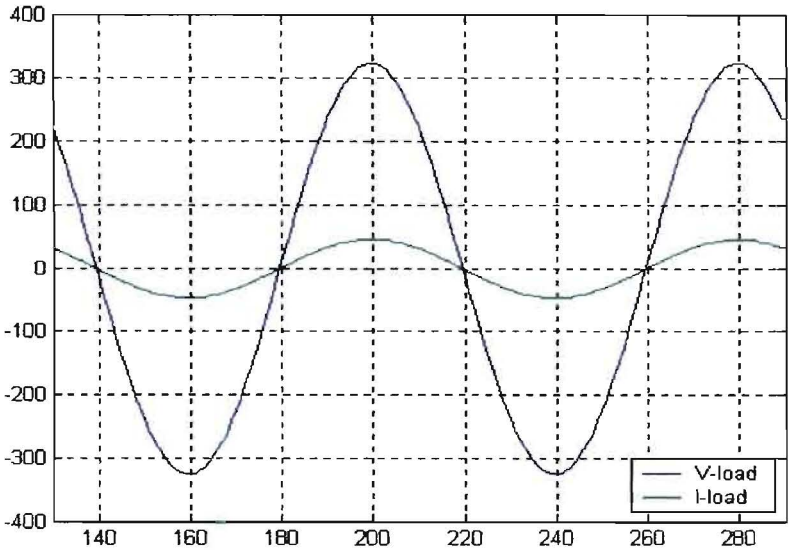


Figure 0-4: V_load and the corresponding current during voltage regulation

The Battery Charging Range

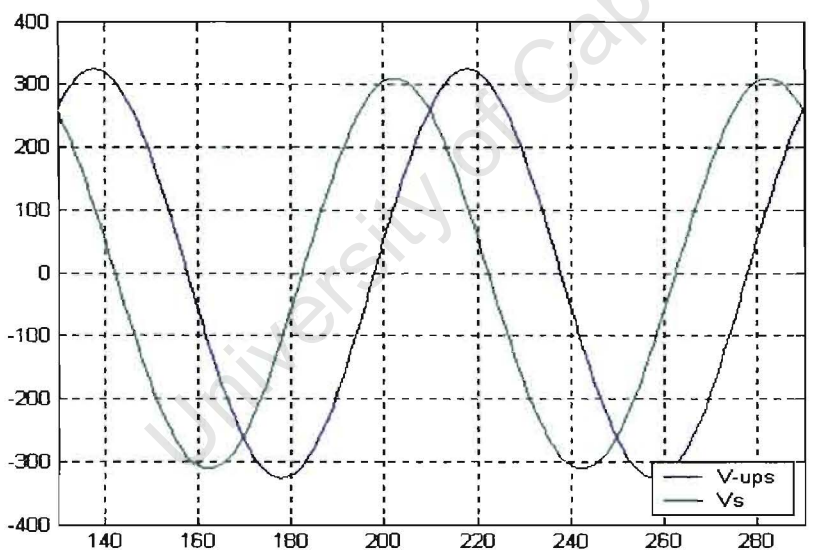


Figure 0-5: V-ups lagging Vs 70 degrees, the battery charging range

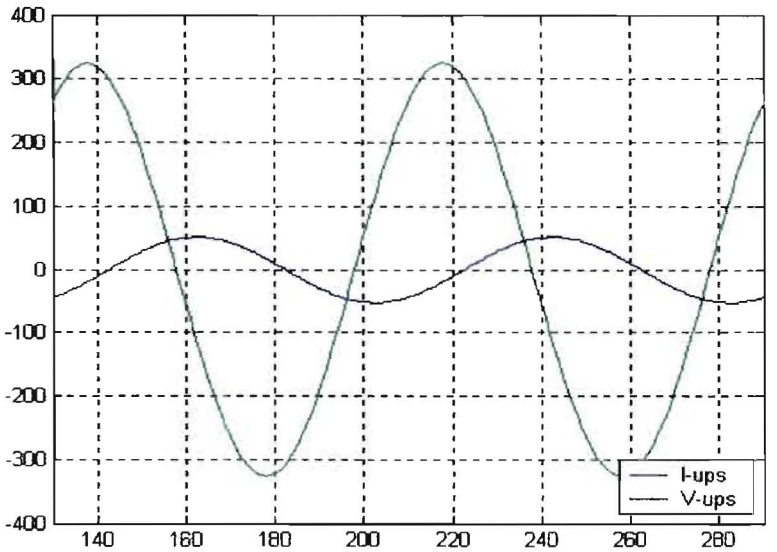


Figure 0-6: Angle between I-ups and V-ups >90 degrees, during battery charging

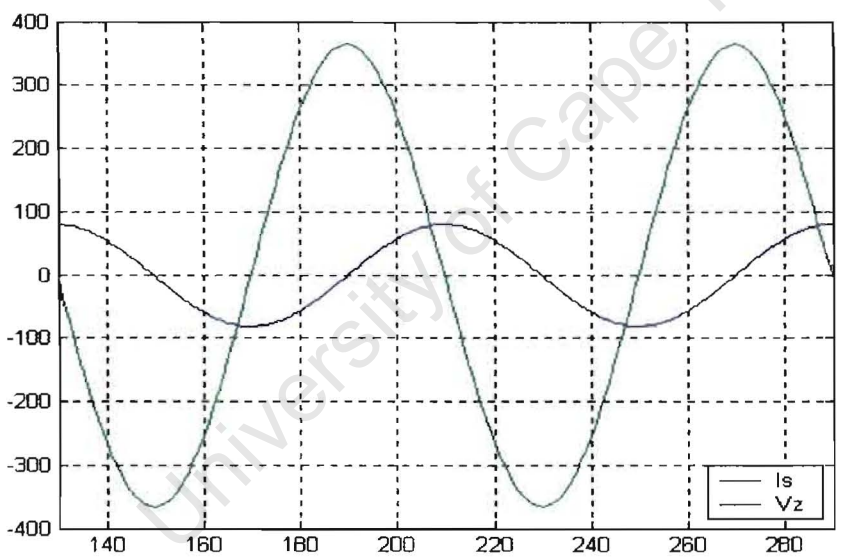


Figure 0-7: Sinusoidal current Is drawn from supply during battery charging

Three Phase Simulations

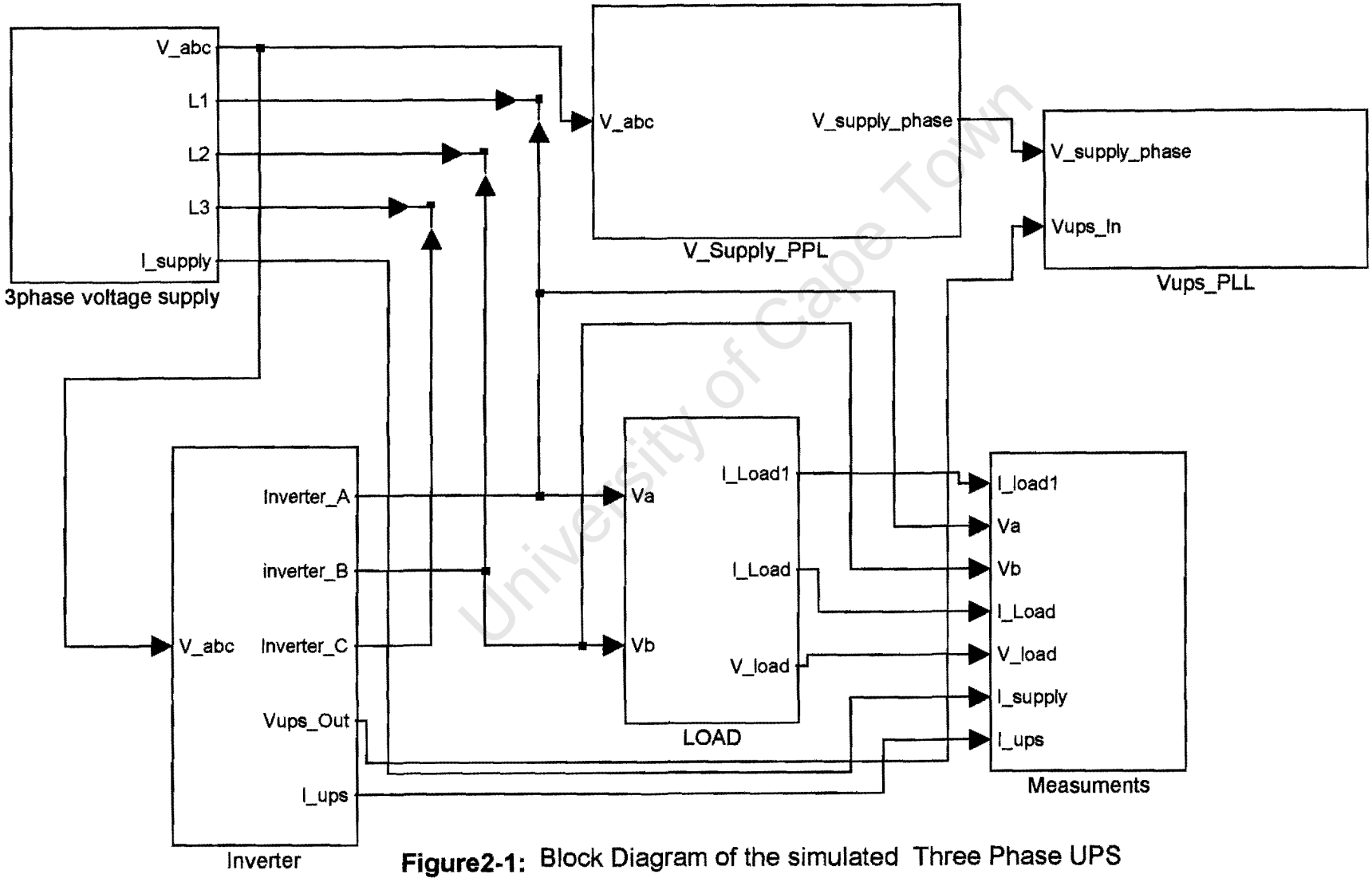


Figure2-1: Block Diagram of the simulated Three Phase UPS

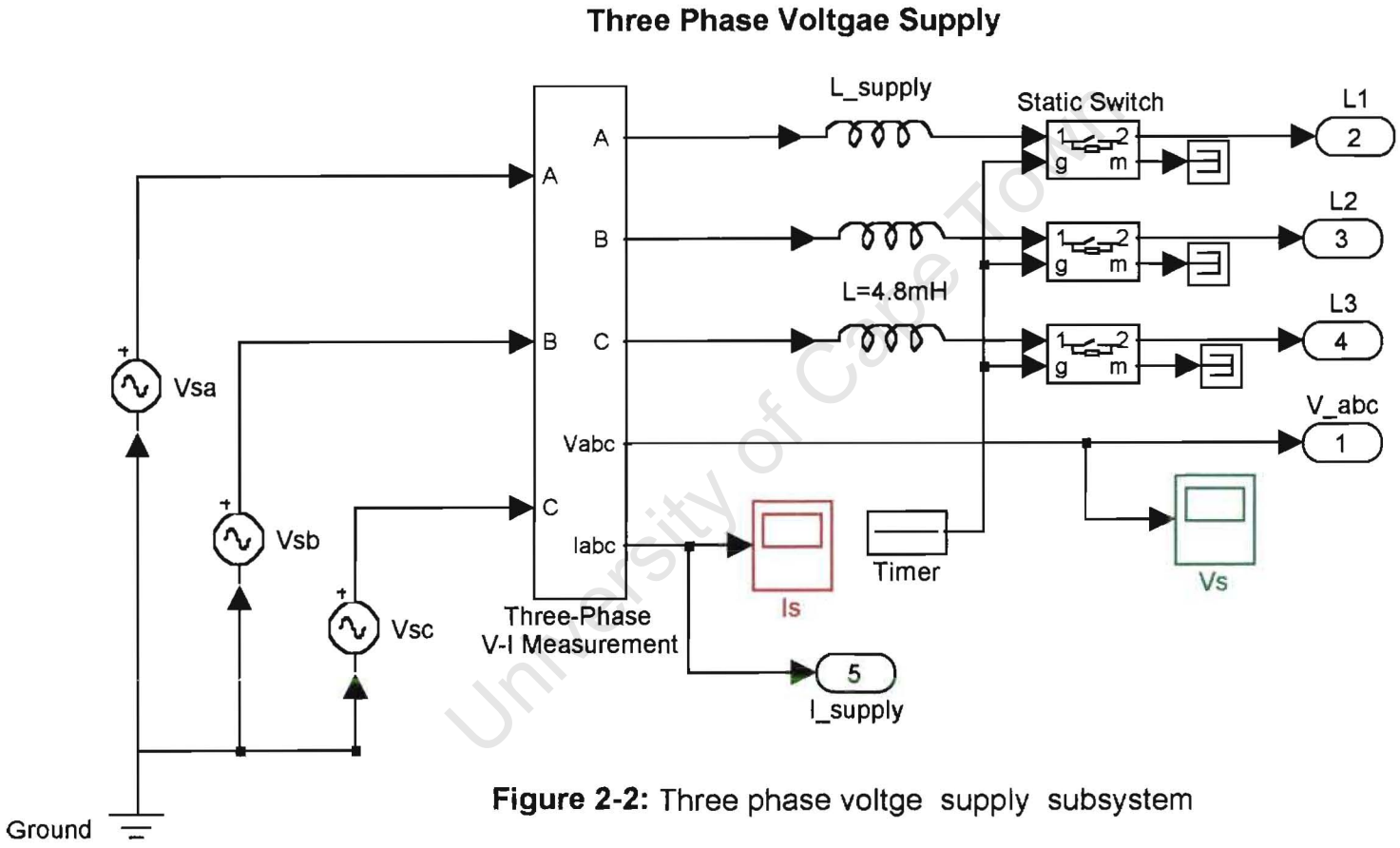


Figure 2-2: Three phase voltge supply subsystem

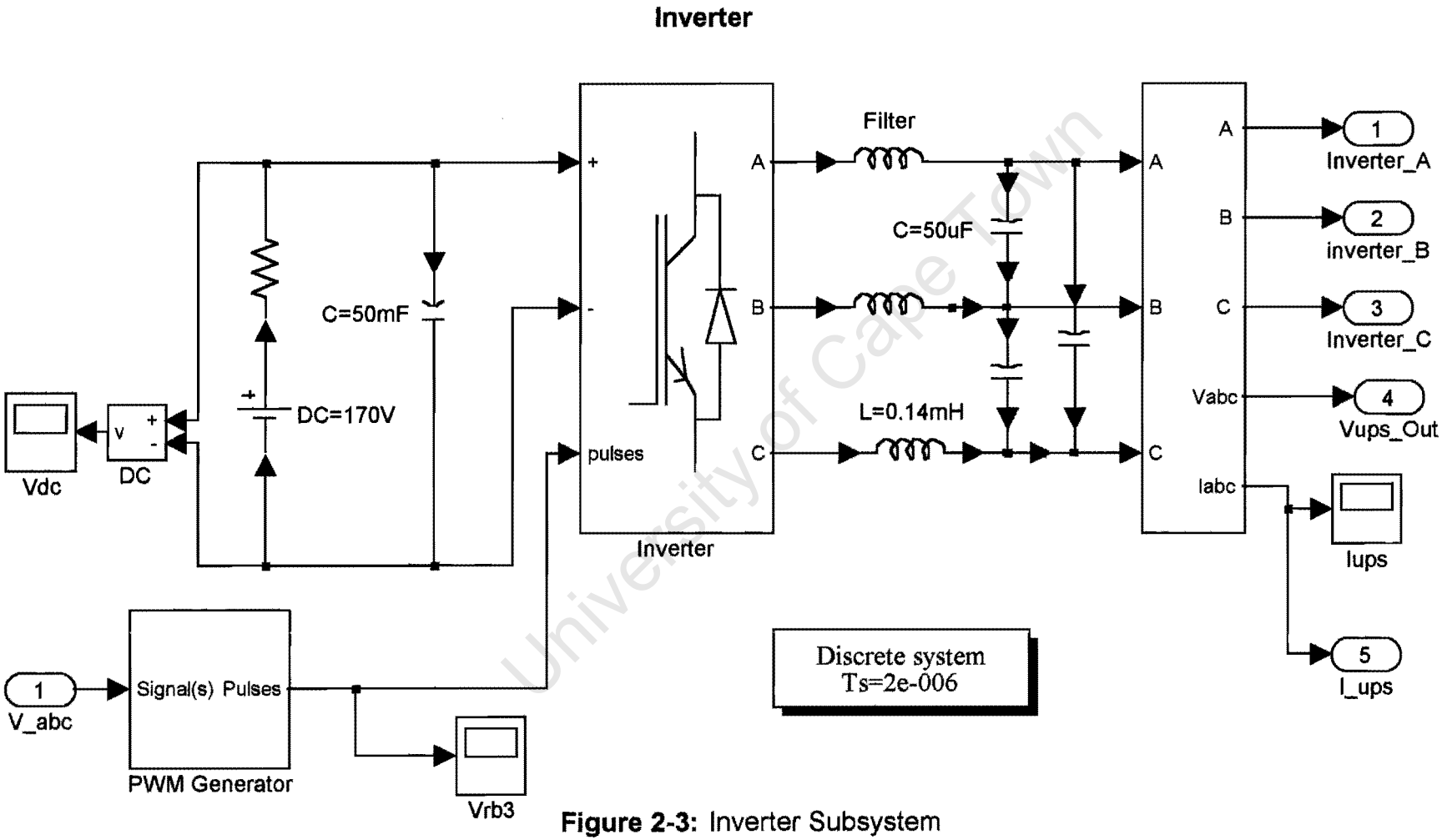


Figure 2-3: Inverter Subsystem

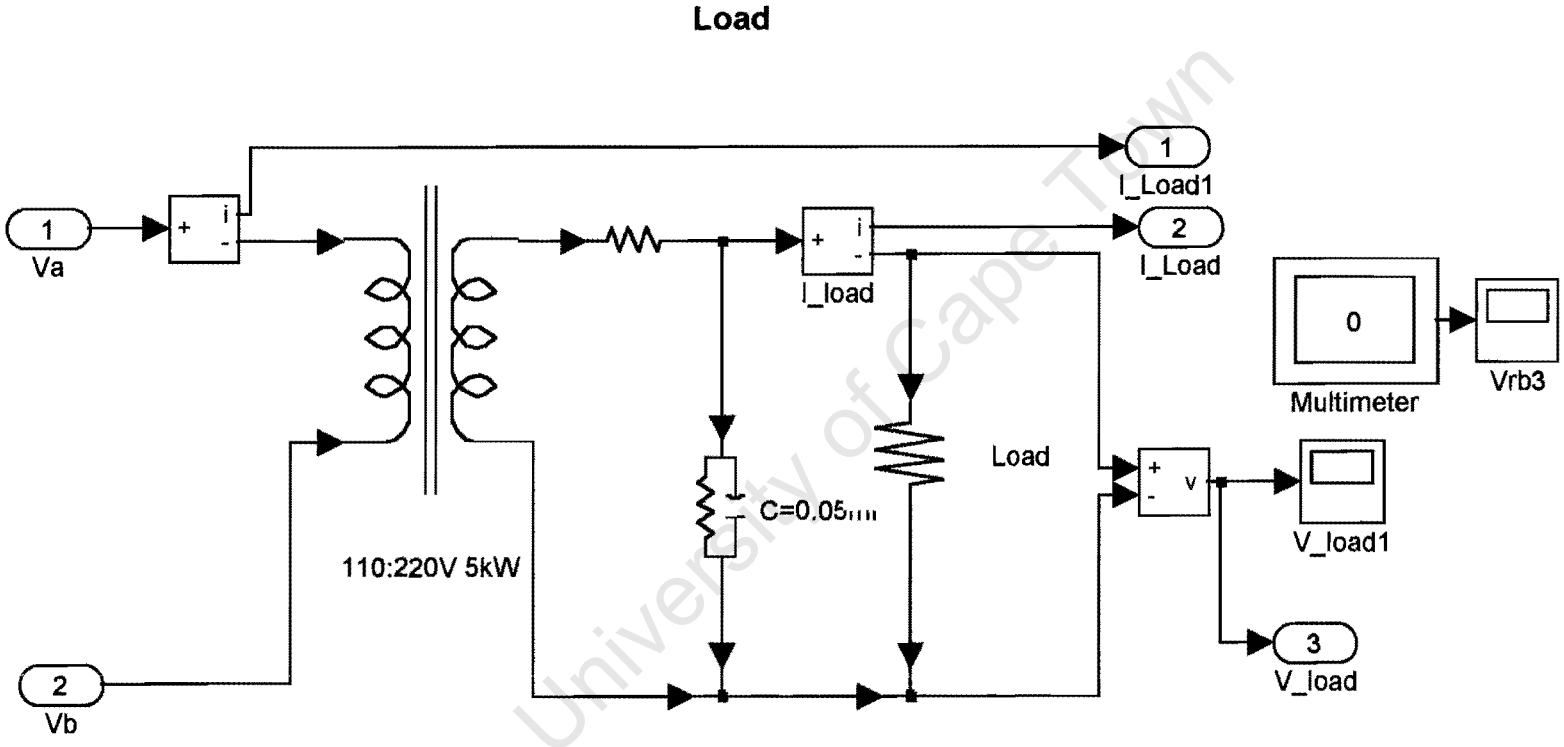


Figure 2-4: Load Subsystem

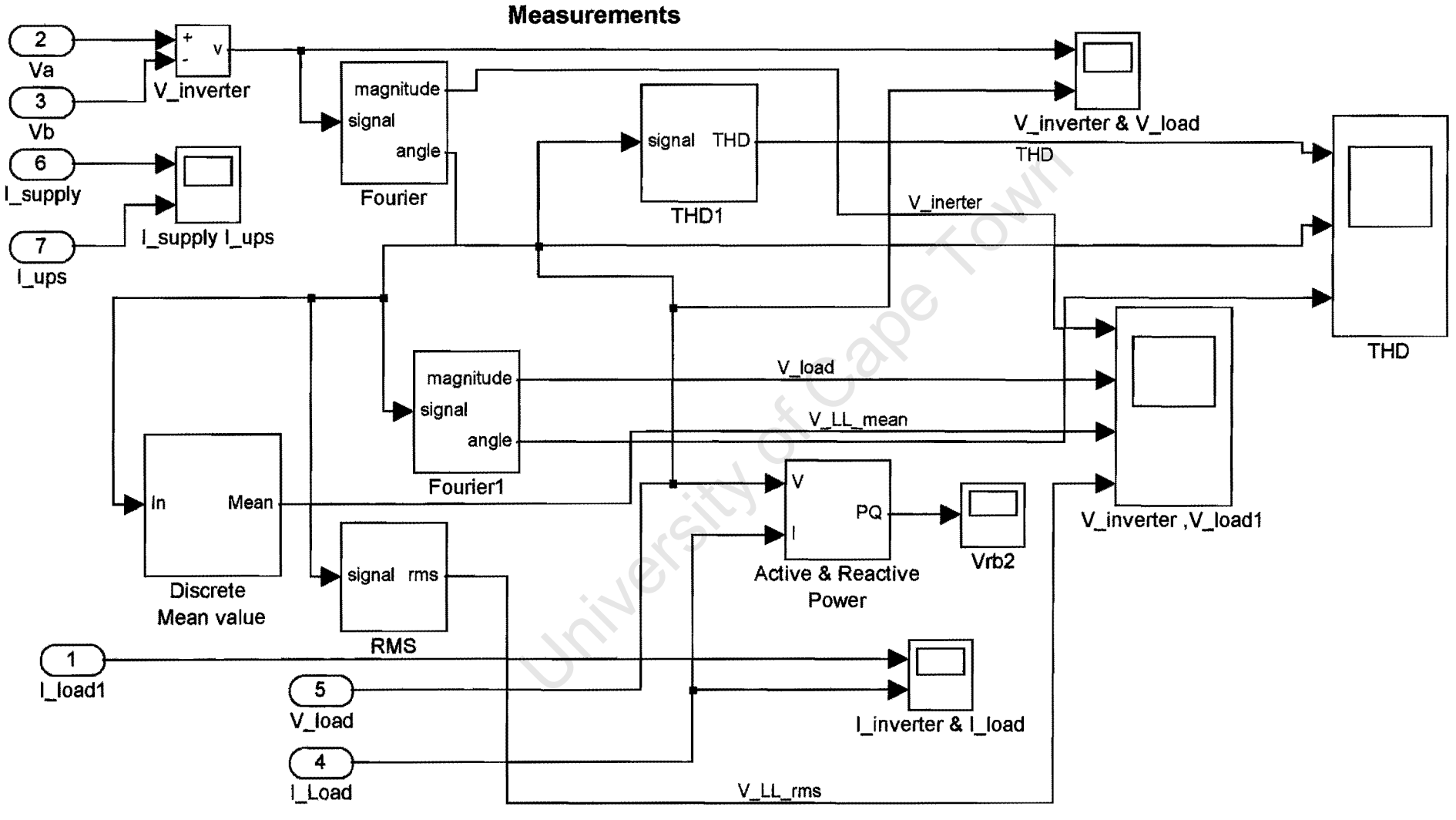


Figure 2-7: Measuments subsystem

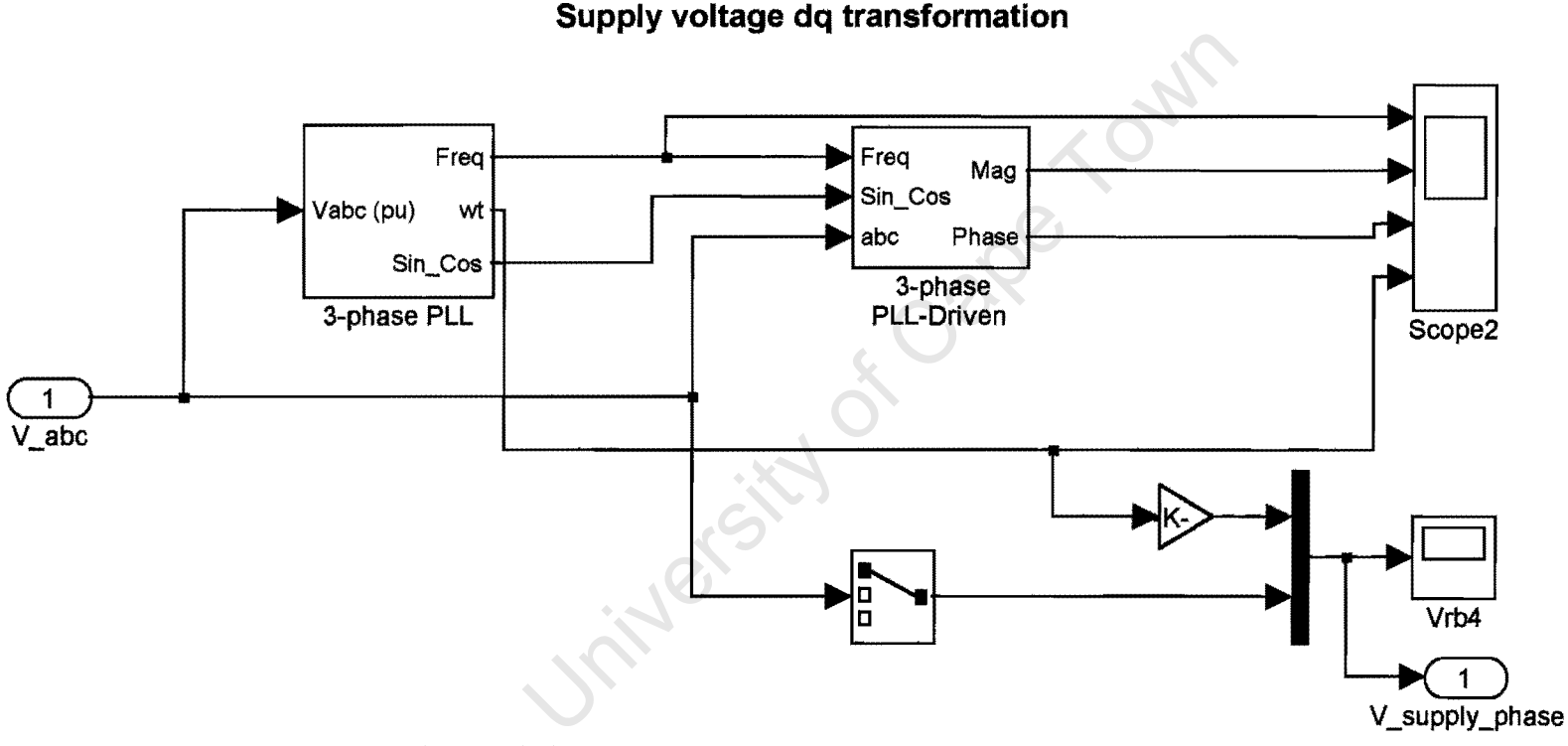


Figure 2-5: Supply voltage dq transformation subsystem

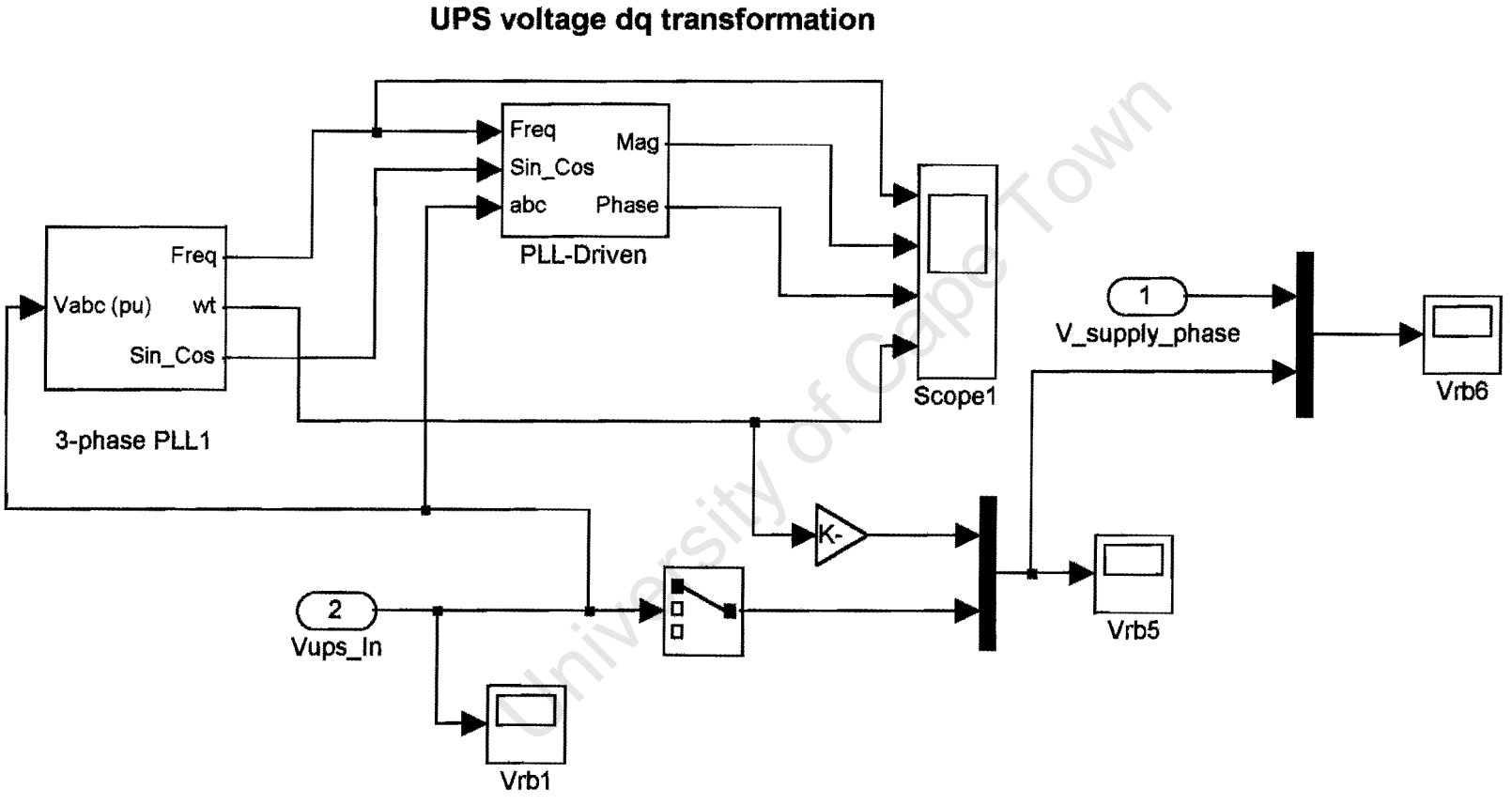


Figure 2-6: V_ups dq transformation subsytem

APPENDIX B

The UCT developed DSP board based on the Texas Instrument TMS320F243

The 243_DSP Development Board

This document will describe the functions of the main components on the 243_DSP Development Board.

Connectors (P1 and P2)

These connectors give access to the input and output pins of the DSP. The tables below describe the function of each pin.

Header 1 (P1)

Header Pin No.	DSP Pin Name	Description		Header Pin No.	DSP Pin	Description
1	N.C	Not Connected		2	N.C	Not Connected
3	PWM1	PWM output pin1		4	PWM2	PWM output pin2
5	PWM3	PWM output pin3		6	PWM4	PWM output pin4
7	PWM5	PWM output pin5		8	PWM6	PWM output pin6
9	IOPD2	Dig. IO pin		10	IOPD3	Dig. IO pin
11	IOPD4	Dig. IO pin		12	T1CMP/IOPB4	Dig. IO pin
13	T2CMP/IOPB5	Dig. IO pin		14	IOPD5	Dig. IO pin
15	TMRDIR/IOPB6	Dig. IO pin		16	TMRCLK/IOPB7	Dig. IO pin
17	QEP1/IOPA3	Dig. IO pin		18	QEP2/IOPA4	Dig. IO pin
19	CAP3/IOPA5	Dig. IO pin		20	IOPD6	Dig. IO pin
21	/PDINT	Power drive Interrupt		22	XINT2/ADCSOC	EXT Int
23	SCIRXD/IOPA1	Dig. IO pin		24	SCITXD/IOPA0	Dig. IO pin
25	5V	5v Power		26	GND	Ground
27	GND	Ground		28	GND	Ground
29	GND	Ground		30	N.C	Not Connected
31	N.C	Not Connected		32	N.C	Not Connected
33	ADCIN0	Ana.-Dig. Conv. Inp.		34	ADCIN1	Ana.-Dig. Conv. Inp.
35	ADCIN2	Ana.-Dig. Conv. Inp.		36	ADCIN3	Ana.-Dig. Conv. Inp.

Header 2 (P2)

Header Pin No.	DSP Pin Name	Description		Header Pin No.	DSP Pin	Description
1	N.C	Not Connected		2	N.C	Not Connected
3	ADCIN4	Ana.-Dig. Conv. Inp.		4	ADCIN5	Ana.-Dig. Conv. Inp.
5	ADCIN6	Ana.-Dig. Conv. Inp.		6	ADCIN7	Ana.-Dig. Conv. Inp.
7	N.C	Not Connected		8	VREFHI	Ref. Voltage
9	GND	Ground		10	GND	Ground
11	N.C	Not Connected		12	N.C	Not Connected
13	N.C	Not Connected		14	N.C	Not Connected
15	GND	Ground		16	GND	Ground
17	N.C	Not Connected		18	N.C	Not Connected
19	N.C	Not Connected		20	N.C	Not Connected
21	5V	5v Power		22	5V	5v Power
23	/RS	Reset		24	N.C	Not Connected
25	CANTX/IOPC6	Dig. IO pin		26	CANRX/IOPC7	Dig. IO pin
27	SPISIMO/IOPC2	Dig. IO pin		28	SPISOMI/IOPC3	Dig. IO pin
29	SPICLK/IOPC4	Dig. IO pin		30	SPISTE/IOPC5	Dig. IO pin
31	IOPD7	Dig. IO pin		32	CLKOUT/IOPD0	Dig. IO pin
33	XF/IOPC0	Dig. IO pin		34	BIO/IOPC1	Dig. IO pin
35	XINT1/IOPA2	Dig. IO pin		36	/NMI	Non Maskable Int.

Programming connectors (J7 and J10)

J7 is for programming the DSP with the JTAG. J10 is a DB9 connector for programming the DSP with the serial port of a computer. To program the DSP, remove jumper J11, switch on the power supply and run the programming software on the computer.
Serial Cable: The serial cable is made up by using a male and a female DB9 connectors. Only pins 2,3,5 and 8 need to be connected.

Jumper Settings

J1 – The voltage reference of the ADC's :
left – External reference voltage.
right – The onboard 5v is used as reference voltage.

J2 – Supply voltage to the FLASH. This jumper can always be in the right position.

J3,J4,J5 – These jumpers should always be connected to supply data to the DAC's

J6 – Jumper connected to run in MC (Micro computer) mode.
____Jumper disconnected to run in MP (Micro processor) mode.

J11 – Serial programming the DSP. (Explained above)

Output of the Digital to Analogue Converters (DAC) (J8)

J8 is the outputs of a 8-channel 8-bit DAC. This is used to display variables inside the DSP on an oscilloscope. This is very useful for debugging DSP code.
IMPORTANT : This is a 8-bit DAC, therefore only values between 0 and 256 is displayed. This means that all variables must be scaled before it can be displayed.

J12 is the power supply (0 – 5 v)
S1 is the reset button.

DSP Software

The directory, DSPShare, contains the DSP software that is used to program the DSP. The DSPShare directory consists of 4 directories – 24xtools, DSPdocumentation, DSPSoftware, Ser243.

Directories :

24xtools – Contains the C-compiler and linker.

DSPdocumentation – Contains the datasheets and the Reference Guide of the TMS320F243 DSP. This is very useful for understanding the F243. Other useful documentation on the F243 can be found on the TI website (www.ti.com)

DSPSoftware – This contains C-code examples and batch files to compile and link C-Code.

Ser243 – Contains the software to program the DSP via the serial connection.

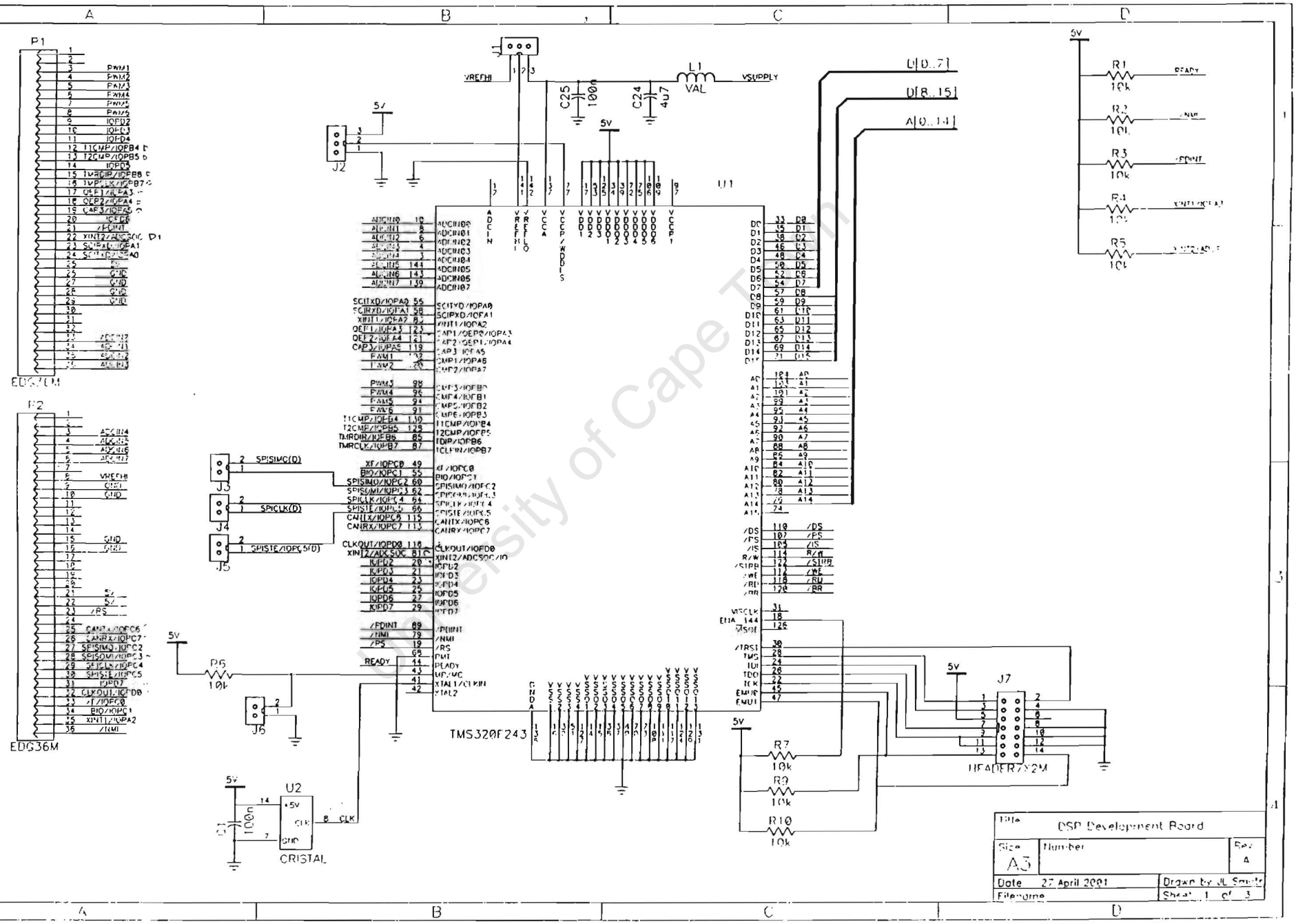
Programming one of the example files

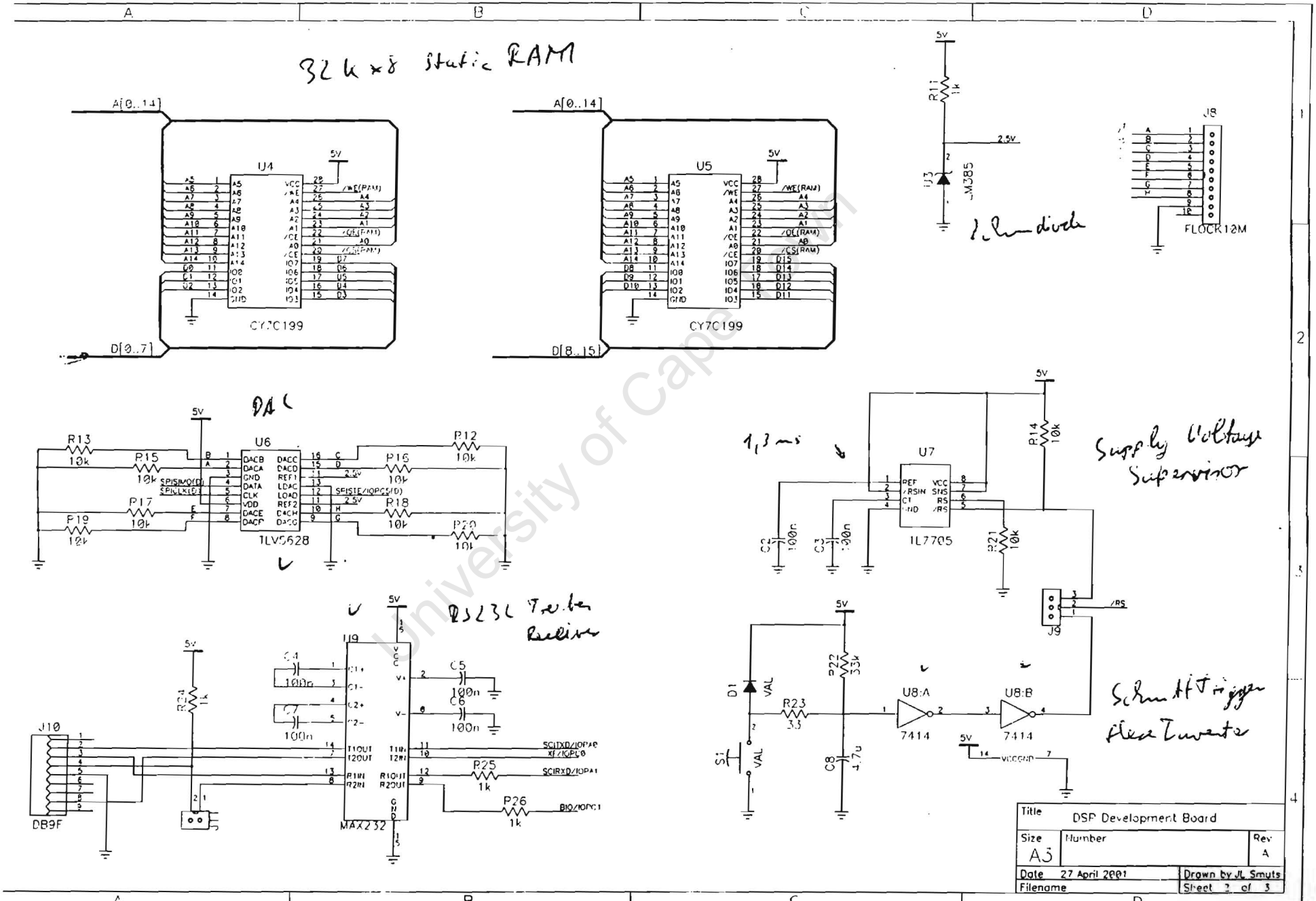
The directory DSPSoftware contains 3 C-code example files :

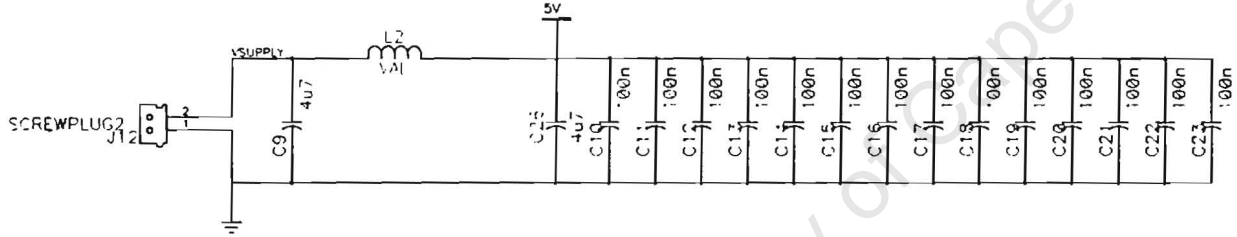
IOPB.c – C-code to produce a square wave on IO Pins IOPB4 – IOPB7.
ADC.c - C-code that read the 3rd ADC channel and writes the value out to DAC1
DAC.c – C-code that displays a counter that count from 0 to 256 on all 8 DACs

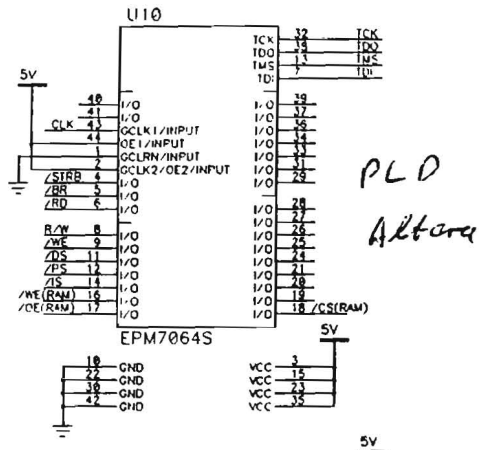
Programming steps.

1. Open one of the example files, make the necessary changes and the save the file as RUN.C, and close the file.
2. Run the batch file named 'Compile.bat'. This will compile and link the C-code and generate a file RUN.OUT.
3. Switch off DSP power, remove Jumper J11 and switch power on again.
4. Change Directory to SER243 and run the 'Con_Prg.bat' file. This will convert the run.out file into a hex format, called run.hex. Then it will programs the DSP trough the serial connection. The serial port for programming can be from COM1 to COM2 by editing the 'Con_Prg.bat' file. Just change the command spf24xb1 to spf24xb2.
5. Switch off power of DSP board, put Jumper J11 on and switch on.
6. Program should be running now, good luck.

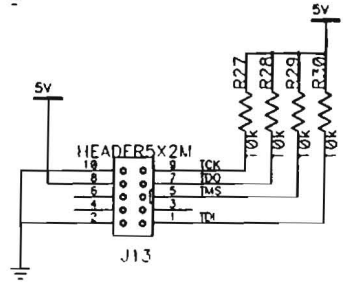








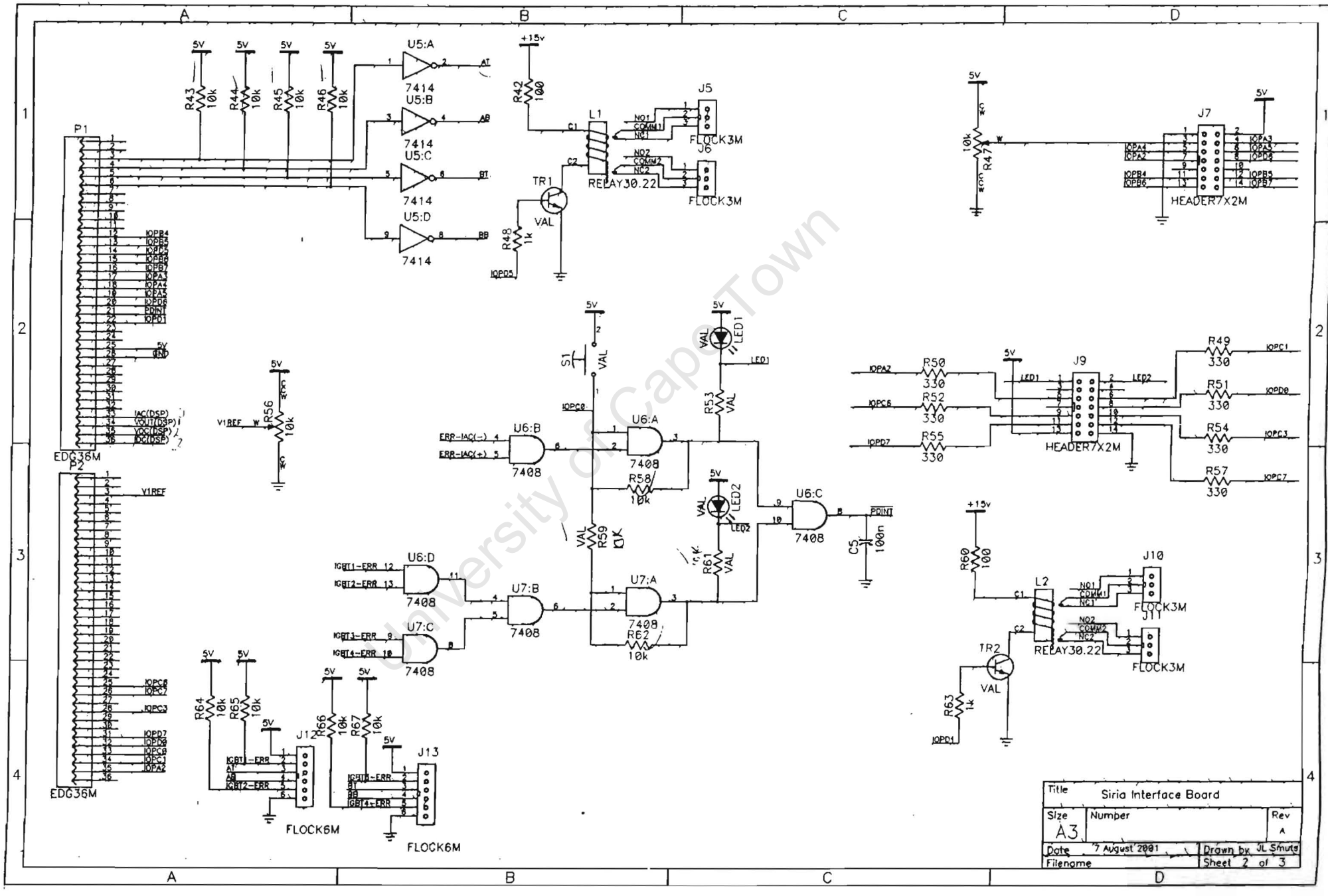
PLD
Altera

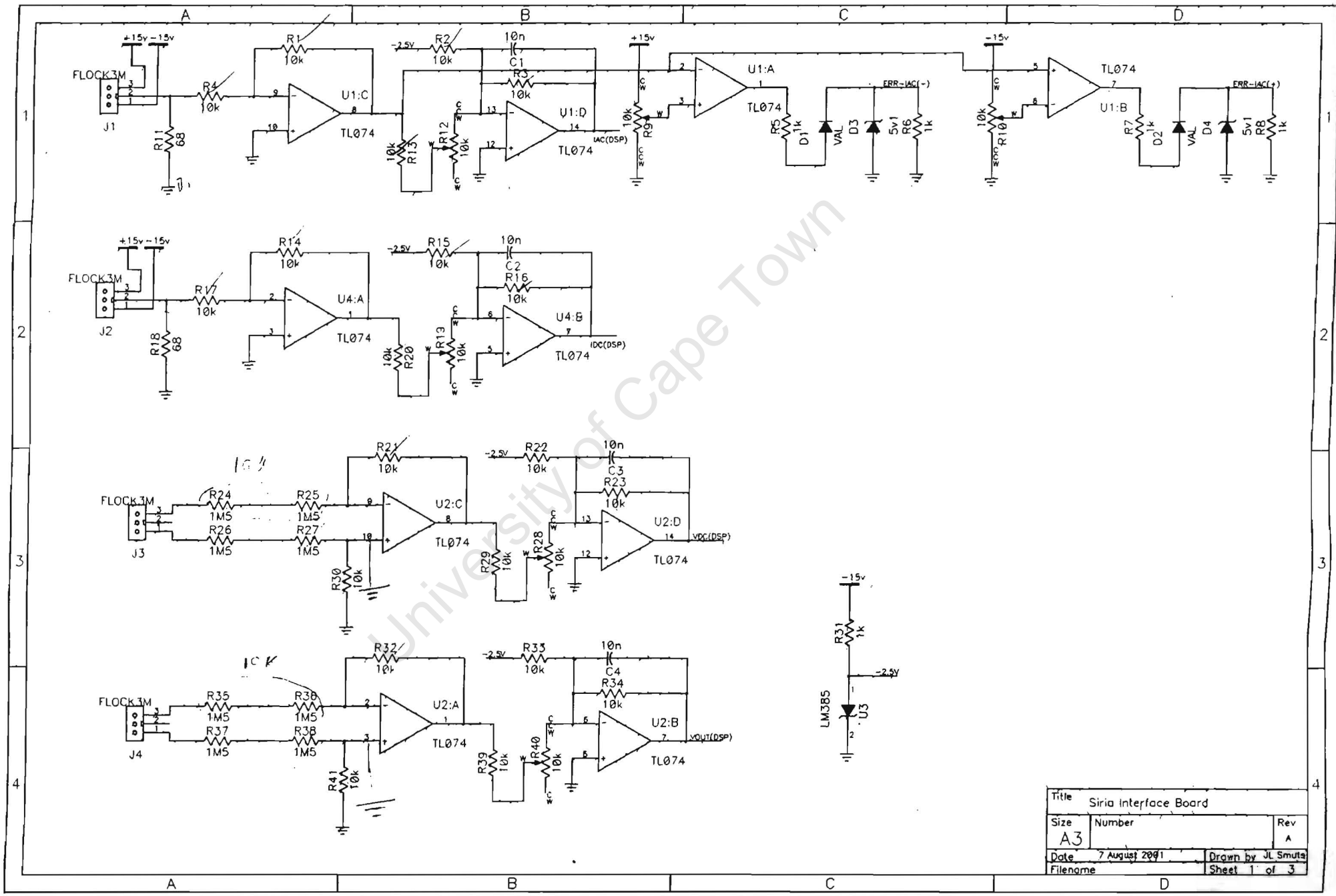


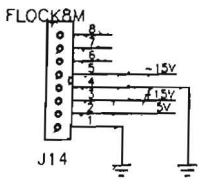
Title	DSP Development Board	
Size A3	Number	Rev A
Date 27 April 2001		Drawn by JL Smuts
Filename		Sheet 3 of 3

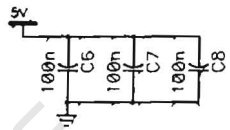
APPENDIX C

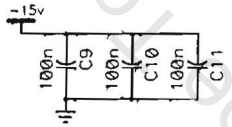
Serial Interface Board

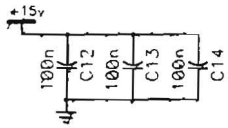








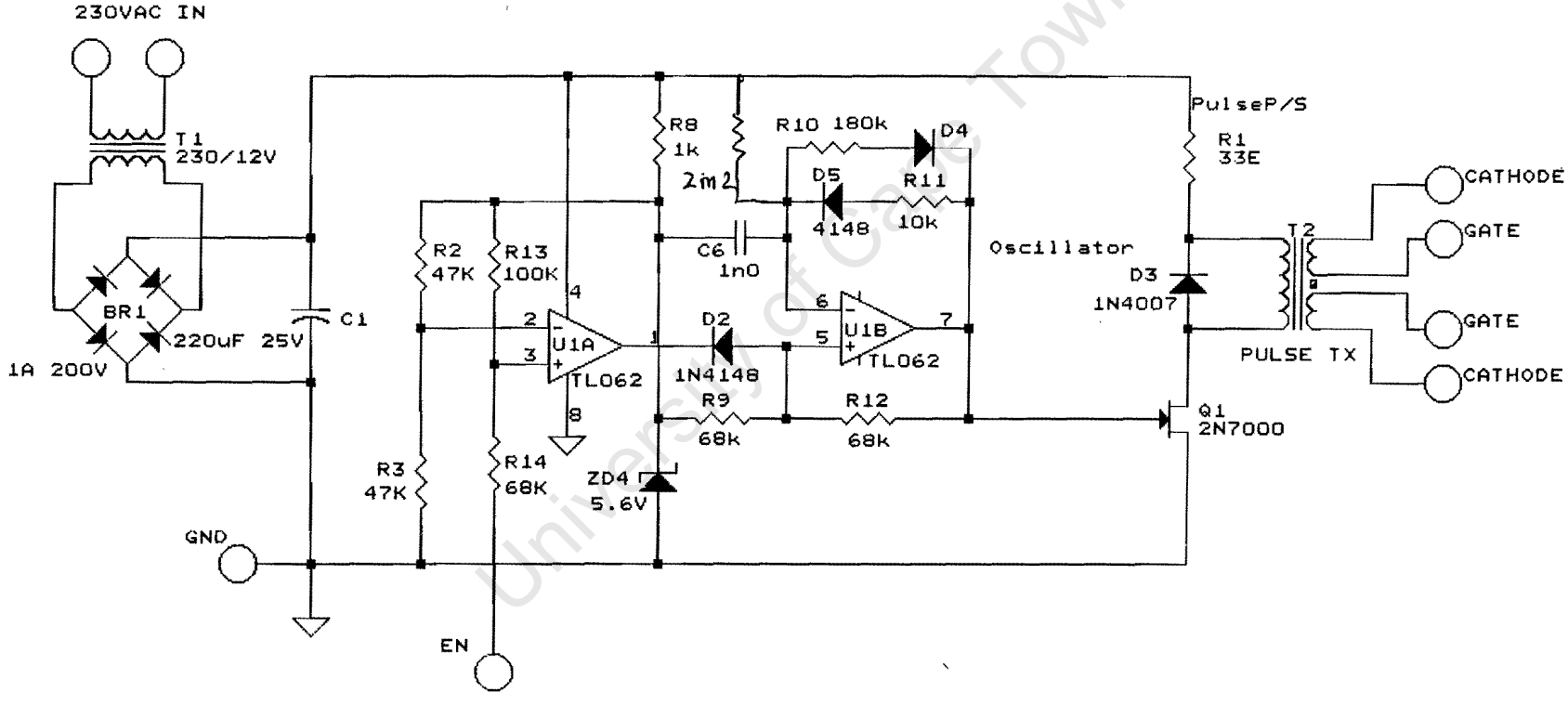




Title	Siria Interface Board		
Size A3	Number		Rev
Date	7 August 2001	Drawn by JL Smuts	
Filename		Sheet 3 of 3	

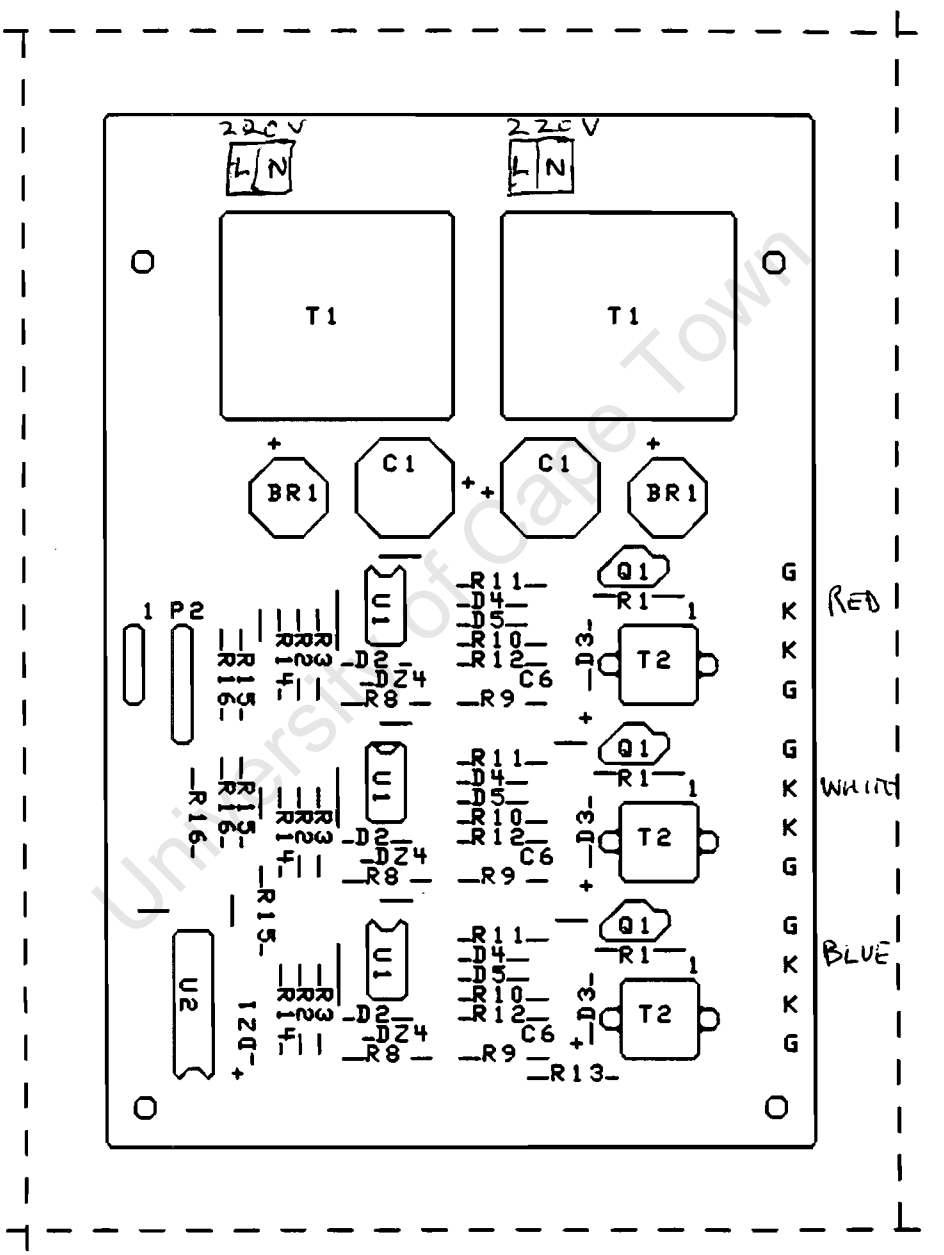
APPENDIX D

Static Switch



Title: STATIC SWITCH		
Size: A	Document Number: STATSW.SCH	REV: 2
Date: January 28, 2002	Sheet 1 of 1	

PIN 1 - GND
PIN 2 - EN RED
PIN 3 - EN WHITE
PIN 6 - EN BLUE



APPENDIX E

Program Code

```
/*************************************************************************/
/** File name:    UPS.c                                                  */
/** Project:      DSP Phase Angle Controlled Three to Single Phase UPS   */
/** Originator:   Caxton Magozore                                        */
/** Target:       TMS320F243                                             */
/*************************************************************************/
/*  Description                                                          */
/*                                                                       */
/*  TMS320F243 is used to implement a closed loop control of a phase  */
/*  angle controlled UPS. The program uses four sensed signals from    */
/*  the UPS to implement control algorithms and generates six space    */
/*  vector PWM for inverter switching. During normal power supply      */
/*  phase angle control is used to regulate the DC bus and charge      */
/*  batteries. On power outage converter only does a pure inverter     */
/*  function. It yields regulated load voltage without considering      */
/*  phase angle control.                                               */
/*************************************************************************/

/* Define Included files       */
#include "F243.h"
#include "float.h"

/*  Peripheral registers and constants of TMS320F243     */
volatile unsigned int *ACTR = (volatile unsigned int *) 0x7413;
volatile unsigned int *DBTCON = (volatile unsigned int *) 0x7415;
volatile unsigned int *COMPR1 = (volatile unsigned int *) 0x7417;
volatile unsigned int *COMPR2 = (volatile unsigned int *) 0x7418;
volatile unsigned int *COMPR3 = (volatile unsigned int *) 0x7419;
volatile unsigned int *COMCON = (volatile unsigned int *) 0x7411;
volatile unsigned int *GPTCON = (volatile unsigned int *) 0x7400;
volatile unsigned int *T1CON = (volatile unsigned int *) 0x7404;
volatile unsigned int *T2CON = (volatile unsigned int *) 0x7408;
volatile unsigned int *OCRA = (volatile unsigned int *) 0x7090;
volatile unsigned int *OCRB = (volatile unsigned int *) 0x7092;
volatile unsigned int *PADATDIR = (volatile unsigned int *) 0x7098;
volatile unsigned int *PBDATDIR = (volatile unsigned int *) 0x709A;
volatile unsigned int *PCDATDIR = (volatile unsigned int *) 0x709C;
volatile unsigned int *PDDATDIR = (volatile unsigned int *) 0x709E;
volatile unsigned int *T1PR = (volatile unsigned int *) 0x7403;
volatile unsigned int *T1CNT = (volatile unsigned int *) 0x7401;
volatile unsigned int *T2PR = (volatile unsigned int *) 0x7407;
volatile unsigned int *T2CNT = (volatile unsigned int *) 0x7405;

volatile unsigned int *EVIMRA = (volatile unsigned int *) 0x742C;
volatile unsigned int *EVIMRB = (volatile unsigned int *) 0x742D;
volatile unsigned int *EVIMRC = (volatile unsigned int *) 0x742E;
volatile unsigned int *EVIFRA = (volatile unsigned int *) 0x742F;
volatile unsigned int *EVIFRB = (volatile unsigned int *) 0x7430;

volatile unsigned int *IMR = (volatile unsigned int *) 0x0004;
volatile unsigned int *IFR = (volatile unsigned int *) 0x0006;

volatile unsigned int *SPICCR = (volatile unsigned int *) 0x7040;
volatile unsigned int *SPICTL = (volatile unsigned int *) 0x7041;
volatile unsigned int *SPISTS = (volatile unsigned int *) 0x7042;
volatile unsigned int *SPIBRR = (volatile unsigned int *) 0x7044;
```

```
volatile unsigned int *SPIRXEMU = (volatile unsigned int *) 0x7046;
volatile unsigned int *SPIRXBUF = (volatile unsigned int *) 0x7047;
volatile unsigned int *SPITXBUF = (volatile unsigned int *) 0x7048;
volatile unsigned int *SPIDAT = (volatile unsigned int *) 0x7049;
volatile unsigned int *SPIPRI = (volatile unsigned int *) 0x704F;
volatile unsigned int *CMPR1 = (volatile unsigned int *) 0x7417; /* Full compare
Registers */
volatile unsigned int *CMPR2 = (volatile unsigned int *) 0x7418;
volatile unsigned int *CMPR3 = (volatile unsigned int *) 0x7419;
volatile unsigned int *XINT2CR = (volatile unsigned int *) 0x7071;

/* Variables      */
int intcount;
int i,k,ia,ib,temp,counter;
int v,va,vb,Vmeas,Vdc;
int Varef,Vbref,Vcref;
int era,Vold,Vload,era_int;
int Aref,Bref,Cref;
int A,B,C,sector;
int Vreal,Vimag,Vmod;
int VoutReal,VoutImag;
int DAC1,DAC2,DAC3,DAC4,DAC5,DAC6,DAC7,DAC8;
int t0,angle_int,Vint,Vsum,cnter;
long int t1,t2;
long int t1temp,t2temp;
int angleout,angle,anglea,angleb,anglec;
int ampcount,amptot,ampavg,ampavg1;
int num,den,Vmod_ave,V_integral;
int clear1,clear2;
int swfr,Vload,Vload_old,upslope;
int delay,programdelay,charcount,screen,diff;

int programfinish,ampltd;



int avgcount,tempavg,Vlo,angle_int_90;
int Imag[70],index;
int angle_Imeas,Iimag;
int angletot,angle_90;
unsigned int count;
int angleold,angle_inc_old;
long int angle_inc,angle_est,era_int_tot;
long int angle_inc_avg,angle_tot,Vload_Int_tot;
int angle_err,angle_add,angle_int_old;

int Vpot,Iinv,Iinv_Int;

long int Vreal_Int_tot,Vload_Int,Iinv_Int_tot;
int Vreal_Int,Vload_ref;
int ampltd_ave;
int amplitude,angle_ref,amplitude_ref;

/* External variables       */
extern int atan();
extern int sine();
extern int invsine();
```

```
/* Determination of quadrant of operation  */
int arctan(int Re,      int Im){
int y1;
      if (Re==0) Re = 1;
      if (Im==0) Im = 1;

      if ((Re>0) & (Im>0))    /* quadrant  1 */
      {
            if (Re>=Im) {y1 = atan((127*Im/Re));}
            else        {y1 = 255 - atan((127*Re/Im));}
            return(y1);
      }

      if ((Im>0) & (Re<0))    /* quadrant 2 */
      {
            if (-Re>=Im)      {y1 = 511 - atan(127*Im/(-Re));}
            else        {y1 = 255 + atan((-127*Re)/Im);}
            return(y1);
      }
      if ((Im<0) & (Re<0))    /* quadrant 3 */
      {
            if (-Re>=-Im)     {y1 = 511 + atan(127*Im/Re);}
            else        {y1 = 767 - atan(127*Re/Im);}
            return(y1);
      }
      if ((Im<0) & (Re>0))    /* quadrant 4 */
      {
            if (-Im>=Re)      {y1 = 767 + atan(127*Re/(-Im));}
            else        {y1 = 1023 - atan((-127*Im)/Re);}
            return(y1);
      }
            }


interrupt void Test1(void)
      {

      }

/*   Timer1 underflow interrupt service routine  */
interrupt void GPT1_underflow(void)
      {

            *PADATDIR |= 0x0004;

            /* Reading Vs and Vdc */

            ADCTRL1 -> ADC1CHSEL = 1;       /* select ADC input 0 */
            ADCTRL1 -> ADC2CHSEL = 2;       /* select ADC input 1 */
            ADCTRL1 -> ADCSOC = 1;         /* start the conversion */
            while (ADCTRL1 -> ADCINTFLAG == 0);
              ADCTRL1 -> ADCINTFLAG = 1;

                  va = *ADCFIFO1;            /* get value from ADC buffer */
                  clear1 = *ADCFIFO1;
                  vb = *ADCFIFO2;             /* get value from ADC buffer */
```

```
                clear2 = *ADCFIFO2;


                va = va>>6;                     /* shift down 6 bits as first 6
bits not used */
                va &= 0x03FF;                   /* make sure bits 10 up are zero
*/
                vb = vb>>6;
                vb &= 0x03FF;

            Vreal = va - 512;               /* shift va to read negative part of Vs
waveform */
            Vdc = vb;                       /* DC bus Vdc */
        Vmeas = 600;                    /* DC bus reference voltage */

      /* Reading V_load and I_battery */

      ADCTRL1 -> ADC1CHSEL = 3;
            ADCTRL1 -> ADC2CHSEL = 0;
            ADCTRL1 -> ADCSOC = 1;
            while (ADCTRL1 -> ADCINTFLAG == 0);
              ADCTRL1 -> ADCINTFLAG = 1;

                va = *ADCFIFO1;
                clear1 = *ADCFIFO1;
                vb = *ADCFIFO2;
                clear2 = *ADCFIFO2;

                va = va>>6;
                va &= 0x03FF;
                vb = vb>>6;
                vb &= 0x03FF;

                Vload = va - 512;
                Iinv = vb - 512;

        angle_int =  *T2CNT/3;          /* internal generated reference angle */

            /* Determining Vs angle  */

            if (index>angle_90) index = 1;
            Vimag = Imag[index];
            Imag[index] = Vreal;
            index++;
            angleold = angle;
            angle = arctan(Vreal/4,Vimag/4);

        if (Vreal_Int<80)  /* checking whether VS is on or off */
            {
                  angle = angle_int;
            Vpot = 0;
            }
            avgcount++;
            count++;

         /* Isolating UPS if Vs off */
      if (Vreal_Int<80)
```

```
            *PDDATDIR &= 0x8000; /* selecting IOPD7 as an output and setting
it low  */
        else *PDDATDIR |= 0x8080;/* selecting IOPD7 as an output and setting it
high  */

            /* Integrating sensed signals  */

            if (Vreal<0) Vreal_Int_tot = Vreal_Int_tot - Vreal;
            else  Vreal_Int_tot = Vreal_Int_tot + Vreal;

        if (Vload<0) Vload_Int_tot = Vload_Int_tot - Vload;
            else Vload_Int_tot = Vload_Int_tot + Vload;

             era_int_tot = era_int_tot + era;

             if (Iinv<0) Iinv_Int_tot = Iinv_Int_tot - Iinv;
            else Iinv_Int_tot = Iinv_Int_tot + Iinv;

            angle_inc_old = angle_inc;


           Vload_ref = 600; /* V_load reference */
               angle_ref = 800;  /* Vdc reference  */

          amplitude_ref = 800; /* amplitude reference */

            /* Averaging the samples and resetting the counter */
            if (((angleold-angle)>500) & (count>angle_90))
                  {     angle_inc = (1023-angleold) + angle;
                        angle_90 = count/4;
                        Vreal_Int = Vreal_Int_tot/count;
                        Vload_Int = Vload_Int_tot/count;
                        era_int = era_int_tot/count;
                        Iinv_Int = Iinv_Int_tot/count;
                        angle_err = 523776 - angle_est;
                        if (angle_err>0) angle_add++;
                        if (angle_err<0) angle_add--;
                        angle_est = 512*angle;
                        Vload_Int_tot = 0;
                        Vreal_Int_tot = 0;
                        era_int_tot = 0;
                        Iinv_Int_tot = 0;
                        count = 0;

                        /* Determine SV PWM amplitude and update the amplitude
*/
                  era = (Vload_ref -(4*Vload_Int));
                        if (era_int>0)
                        { if (era>10) ampltd = ampltd +5;
                           else ampltd++;
                        }
                        if (era_int<0)
                        {  if ( era <-10)ampltd = ampltd-5;
                            else ampltd--;
                        }
                        if (ampltd>280) ampltd = 280;
                        if (ampltd<0) ampltd = 0;
```

```
                amplitude = ampltd;
        }


    else angle_inc = angle - angleold;

    angle_tot = angle_tot + 512*angle_inc;


/* Determine phase shift angle and updating phase shift angle */
    if (Vreal_Int>80)
    {
            if (counter == 10)
    {
        diff = angle_ref/4 - Vdc/4;
              if ((diff>0)&&(((Iinv_Int)*2)<Vmeas)) Vpot++;
              if ((diff<0 )||(((Iinv_Int)*2)>Vmeas)) Vpot--;
              if (Vpot>90 && diff>0) Vpot = 90;
              if (Vpot<0) Vpot = 0;

              counter = 0;
    }

    }

    if (avgcount>2046)

     {
             angle_inc_avg =  angle_tot/2048;
               angle_tot=0;
               avgcount =0;
        }


    angle_est = angle_est + angle_inc_avg + angle_add;
    angleout = angle_est/512;




    if (angleout>1023) angleout = angleout - 1023;


    anglea = angleout + 658 - Vpot;   /* Reference angle phase A */

    if (anglea>1023) { anglea = anglea - 1023;}
 if (anglea<0) { anglea = anglea + 1023; }
    Varef = sine(anglea);          /* reference sine wave A */

    angleb = anglea + 682;           /* Reference angle phase B */
    if (angleb>1023) { angleb = angleb - 1023; }
 if (angleb<0) { angleb = angleb + 1023; }
    Vbref = sine(angleb);             /* reference sine wave B */


    anglec = anglea + 341;          /* Reference angle phase C */
```

```
if (anglec>1023) { anglec = anglec - 1023; }
if (anglec<0) { anglec = anglec + 1023; }
Vcref = sine(anglec);              /* reference sine wave C */

/* Determining sector for space vector modulation */
if (Varef>Vbref) {A = 1;}
else {A = 0;}
if (Vbref>Vcref) {B = 1;}
else {B = 0;}
if (Vcref>Varef) {C = 1;}
else {C = 0;}

sector = A + 2*B + 4*C;

/* Determine switching times T2, T1 and T0 */
if (sector==3)
      {t1temp = Varef - Vbref;
       t1 = (amplitude*t1temp)/512;
       t2temp = -Vcref + Vbref;
       t2 = (amplitude*t2temp)/512;
       t0 = swfr - t1 - t2;
       Aref = t0/2;
       Bref = t0/2 + t1;
       Cref = t0/2 + t1 + t2;
      }
if (sector==2)
      {t2temp = -Vcref + Varef;
       t2 = (amplitude*t2temp)/512;
       t1temp = Vbref - Varef;
       t1 = (amplitude*t1temp)/512;
       t0 = swfr - t1 - t2;
       Bref = t0/2;
       Aref = t0/2 + t1;
       Cref = t0/2 + t1 + t2;
      }
if (sector==6)
      {t1temp = Vbref - Vcref;
       t1 = (amplitude*t1temp)/512;
       t2temp = -Varef + Vcref;
       t2 = (amplitude*t2temp)/512;
       t0 = swfr - t1 - t2;
       Bref = t0/2;
       Cref = t0/2 + t1;
       Aref = t0/2 + t1 + t2;
       }
if (sector==4)
      {t2temp = -Varef + Vbref;
       t2 = (amplitude*t2temp)/512;
       t1temp = Vcref - Vbref;
       t1 = (amplitude*t1temp)/512;
       t0 = swfr - t1 - t2;
       Cref = t0/2;
       Bref = t0/2 + t1;
       Aref = t0/2 + t1 + t2;
      }
if (sector==5)
      {t1temp = Vcref - Varef;
```

```
            t1 = (amplitude*t1temp)/512;
            t2temp = -Vbref + Varef;
            t2 = (amplitude*t2temp)/512;
            t0 = swfr - t1 - t2;
            Cref = t0/2;
            Aref = t0/2 + t1;
            Bref = t0/2 + t1 + t2;
           }
   if (sector==1)
           {t2temp = -Vbref + Vcref;
            t2 = (amplitude*t2temp)/512;
            t1temp = Varef - Vcref;
            t1 = (amplitude*t1temp)/512;
            t0 = swfr - t1 - t2;
            Aref = t0/2;
            Cref = t0/2 + t1;
            Bref = t0/2 + t1 + t2;
           }

   /* Apply switching times to compare registers */
   *COMPR1 = Aref;
   *COMPR2 = Bref;
   *COMPR3 = Cref;

/* Debugging */

          DAC1 = Vreal/4 + 128;     /* Vreal/4 + 128*/
          DAC1 = DAC1<<4;
          DAC1 &= 0x0FFF;
          DAC1 |= 0x0000;

          *SPITXBUF = DAC1;
          for (i=0; i<4; i++)
               {}
          *PCDATDIR &= 0x0FFDF;
          *PCDATDIR |= 0x0020;



          DAC2 = Vimag/4 + 128;    /* Vimag/4 + 128,*/
          DAC2 = DAC2<<4;
          DAC2 &= 0x0FFF;
          DAC2 |= 0x2000;

          *SPITXBUF = DAC2;
          for (i=0; i<4; i++)
               {}
          *PCDATDIR &= 0x0FFDF;
          *PCDATDIR |= 0x0020;



          DAC3 = anglea/4;  /* angle/4 */
          DAC3 = DAC3<<4;
          DAC3 &= 0x0FFF;
          DAC3 |= 0x4000;
```

```
*SPITXBUF = DAC3;
for (i=0; i<4; i++)
      {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC4 = angleb/4;  /* angleout/4 */
DAC4 = DAC4<<4;
DAC4 &= 0x0FFF;
DAC4 |= 0x6000;

*SPITXBUF = DAC4;
for (i=0; i<4; i++)
      {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC5 = Vdc/4;           /* Varef/8 + 128 */

DAC5 = DAC5<<4;
DAC5 &= 0x0FFF;
DAC5 |= 0x8000;

*SPITXBUF = DAC5;
for (i=0; i<4; i++)
      {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC6 =  angle_ref/4;          /* Vbref/8 + 128*/
DAC6 = DAC6<<4;
DAC6 &= 0x0FFF;
DAC6 |= 0xA000;

*SPITXBUF = DAC6;
for (i=0; i<4; i++)
      {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC7 = (4*Vload_Int);   /* Vcref/8 + 128 */
DAC7 = DAC7<<4;
DAC7 &= 0x0FFF;
DAC7 |= 0xC000;

*SPITXBUF = DAC7;
for (i=0; i<4; i++)
      {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC8 = Vload_ref/4;
DAC8 = DAC8<<4;
DAC8 &= 0x0FFF;
DAC8 |= 0xE000;
```

```
                *SPITXBUF = DAC8;
                for (i=0; i<4; i++)
                      {}
                *PCDATDIR &= 0x0FFDF;
                *PCDATDIR |= 0x0020;


                for (i=0; i<100; i++)
                      {}

                *PADATDIR &= 0xFFFB;

                programfinish = 1;
                *EVIFRA |= 0x0200;

                counter++;
          }

interrupt void Test3(void)
      {
      }

interrupt void Test4(void)
      {
      }

interrupt void Test5(void)
      {
      }

interrupt void XINT2(void)
      {

      }

/* Main background loop starts here */
void main(void)
      {

            *PADATDIR &= 0xFF00; /* configuring PADATDIR */

            *IMR = 0x0022;         /* Masking and unmasking registers */
            *IFR = 0xFFFF;
            *EVIMRA = 0x0201;       /* T1 UNFINT enable */
            *XINT2CR |=0x0003;
            *XINT2CR &=0xFFFB;

            asm(" clrc INTM");


ADCTRL2 -> ADCPSCALE = 3;  /* Pre-scale value = 8 */
ADCTRL2 -> ADCEVSOC = 0;
ADCTRL2 -> ADCEXTSOC = 0;

ADCTRL1 -> ADCIMSTART = 0;
ADCTRL1 -> ADCINTEN = 0;   /* disable interrupt */
ADCTRL1 -> ADCCONRUN = 0;  /* single conversion */
```

```
ADCTRL1 -> ADC2EN = 1;      /* en/dis(0)-able ADC2 */
ADCTRL1 -> ADC1EN = 1;      /* enable ADC1 */

ADCTRL1 -> suspend_free = 0;
ADCTRL1 -> suspend_soft = 1;

/* SPI port setup for DAC coms */

      *SPICCR &= 0x0FF7F; /* reset */
      *OCRB |= 0x001C;  /* not GPIO but SPISIMO, SPISOMI, SPICLK */
      *SPICCR |= 0x000B;       /* char length = 12 */
      *SPICTL = 0x0006; /* master, enabled TX, int disabled */
      *SPIBRR |= 0x0003;       /* set baud rate */
      *SPICCR |= 0x0080;       /* ready */

      *PCDATDIR |= 0x2020;     /* IOPC5 is high (load)*/
    *PADATDIR |= 0x0400;       /* PA2 Output for cycle measure */

      /* registers for PWM generation */

      *OCRA |= 0x0FC0;  /* enable compare pins rather than GPIO */
      *ACTR = 0x0999;    /* active low, active high, then passed through
inverter on i/o board*/
      *DBTCON = 0x00E0;/* dead band of 0 clock cycles  = 0nsec */
      *OCRB |=0x0003;   /* selecting IOPC0 and IOPC1 as out puts */
      *PCDATDIR |= 0x0101;

      *COMPR1 = 0;
      *COMPR2 = 0;

      *COMCON = 0x0307;
      *COMCON = 0x8307;

      swfr = 1024;
      *T1PR = swfr;  /* Period = 1024*50nsec*2 = 100usec : freq approx 10kHz */
      *T1CNT = 0x0;   /* Initialised to zero to ensure timer 1 starts counting
from zero */
      *T1CON = 0xA802;   /* up/down continuous mode */

      *T2PR = 3069;    /* Period = 3069*50nsec*128 approx = 20msec or 50Hz */
      *T2CNT = 0x0; /* Initialised to zero to ensure timer 2 starts counting
from zero */
      *T2CON = 0x9702;   /* set in cont up, and set clock prescaler to 128 */

      *T1CON = 0xA842;   /* start the clock */
      *T2CON = 0x9742;   /* start the clock */

      /*Initialise variables  */
            angle = 0;
            angleout = 0;
            angle_add = 0;
            programfinish = 0;
            screen = 1;
            index = 1;
            count = 0;
            Vmod = 0;
            angle_int = 0;
```

```
        era = 0;
        angle_int_old = 0;
        Vsum = 0;
        cnter = 0;
        diff = 0;
        avgcount = 1;
        Vreal_Int_tot = 0;

        angle_90 = 25;

}
```